Two Dimensional Analytical Subthreshold Model of Nanoscale Cylindrical Surrounding Gate MOSFET Including Impact of Localised Charges

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The paper presents a two dimensional analytical subthreshold model of Nanoscale Cylindrical Surrounding Gate (SRG) MOSFET with localised/fixed interface charges. The model is used to study the effect of localised charges induced at the semiconductor/oxide interface due to the hot carrier induced damage, stress induced damage or radiation induced damage on the electrical performance of the device. The device reliability issues of Nanoscale Cylindrical SRG MOSFETs under localised interface charges are also studied and effects of extension, position, density and polarity of interface localised charges are discussed in detail in terms of change in potential, threshold voltage shift, drain current degradation.

Keywords: ATLAS-3D, Hot Carrier Effect, Interface Traps, Localised Charges, SRG MOSFET.

1. INTRODUCTION

Nanowire or nanoscale Cylindrical Surrounding-Gate (SRG) MOSFET has been recognized as one of the possible choices to boost CMOS performance boost beyond the conventional scaling limit.1 In principle, Surrounding-gate MOSFET can provide the best controllability of short-channel effects (SCEs),2 which are the predominant factors that limit how far a MOSFET can be scaled down. Nanoscale cylindrical SRG MOSFET is one of the most promising device architecture to extend CMOS scaling, as it provides enhanced electrostatic control of the channel.3,4 Historically, devices have been scaled to improve device and circuit performance but a major concern is long term reliability. The evaluation of long term reliability of MOS VLSI circuits is becoming more important as the complexity and density of VLSI chips increase. So circuit reliability issues need to be addressed rigorously in the early design phase. There are many factors responsible for the device damage problems. The most important are: (1) process induced,5 (2) stress induced damage,6 (3) radiation induced damage7 and (4) hot carrier induced damage.8 For MOS technologies, ionizing radiation generally increases the positive oxide charge density and interface state density which causes threshold voltage shift and transconductance degradation. Stress induced damage can be two types: electrical stress and processing damage i.e., induced by plasma etching.6 The need for sub-100 nm devices in CMOS circuitry necessitates the use of plasma etching for pattern transfer processes. However, the damage to the gate oxide and oxide/Si interface induced by plasma etching can adversely affect yield, performance and reliability. The degradation of MOSFET characteristics due to the injection of hot carriers in the gate oxide stands as one of the most important challenges to further progress of device down-scaling. The hot-carrier effect is mainly caused by the high electric field in the channel near the drain junction which provides enough energy to the channel electrons which may generate electron-hole pairs through impact ionization. The generated holes are attracted to the substrate to form the substrate current and the electrons are swept toward to the drain. If the electrons get enough energy to reach the Si–SiO2 interface and surmount the barrier, gate current is resulted. This gate current more or less creates damage in the oxide or on the interface near the drain junction and device performance is degraded. In past three decades, a lot of work has been focused on the hot-carrier degradation of conventional MOS transistors.9–13
The damage is commonly believed to result in (a) charge trapping in the gate oxide\textsuperscript{12} and (b) interface-state generation at the Si–SiO\textsubscript{2} interface.\textsuperscript{13,14} Recently, hot carrier effect has been studied in SOI MOSFET\textsuperscript{15,16} and p-gate \textit{p}-MOSFET.\textsuperscript{17} All types of damages result in induced localised charges at the Si–SiO\textsubscript{2} interface. The localised interface charges induced is summarized in the formation of a narrow defective interface region. The interface trap or oxide-trapped charges which exist at the semiconductor/oxide interface can be transformed into equivalent localised interface charges. A lot of research work has been done to study the effect of localised charges on SRG MOSFET.\textsuperscript{18–21} Previous models model did not incorporate SCE and have assumed a parabolic surface potential profile which may not be useful for sub-90 nm gate lengths. Further the effect of localised charges on subthreshold current, subthreshold slope and DIBL have not been studied which are extremely important for sub-100 nm devices.

In this paper, we have used Evanescent Mode Analysis (EMA) technique which suits well for Nanoscale Surrounding Gate (SRG) MOSFET. Cylindrical coordinates have been used to solve the Poisson’s equation which is appropriate for finding the solution for the cylindrical geometry. To characterize the damage induced localised charges, one usually measures it in terms of the change in potential, threshold-voltage shift, drain current and transconductance degradation. This work is an indicative study which is useful to study the behavior of localised charges and their effect on the device performance. Bouhdada et al.\textsuperscript{22} presented a threshold voltage variation model for a stressed MOSFET with a Gaussian distribution for the interface charges. While the Gaussian function yields a better approximation of the defect distribution, such a model is quite complex. To develop a simplistic analytical model, we have employed the step-function approximation for the interface charge distribution. The effect of density of localised interface charges (positive and negative), length of damaged region and position of damaged region on the device characteristics (Potential, Conduction band energy, Valence band energy, Threshold Voltage, Subthreshold current and Subthreshold slope) has been analyzed and exhaustive simulation have been done using 3-D device simulator\textsuperscript{23} to validate the analytical results. Apart from giving deep insight into the device physics, the analytical results are useful in predictive compact subthreshold modeling of SRG MOSFET. We have used radius of the silicon pillar \((R) > 5\) nm and thus quantum mechanical effects (QME) can be neglected\textsuperscript{24} without compromising the accuracy of the results.

2. MODEL DESCRIPTIONS

Figure 1 shows the schematic cross section of the simulated Nanowire MOSFET structure with localised interface charges. The models activated in simulation comprises of field dependent mobility, concentration dependent mobility model along with the Shockley–Read–Hall (SRH) recombination models for minority carrier recombination. Density of localised charges has been set using the QF parameter in the INTERFACE statement. In order to study the effect of location and extension of localised charges, we have divided the damaged device into three regions and the surface potential is obtained by solving the two-dimensional (2-D) Poisson’s equation separately in three regions and applying potential and field continuity conditions at interface of three regions, i.e., \(L_2\) (length of damaged region), \(L_3\) (distance of damaged region from drain) \(L_1\) (damage free part i.e., \(L - L_2 - L_3\)).

To solve for potential distribution in Silicon film, we start with the Poisson equation in cylindrical coordinates as:

\[
\frac{1}{r} \frac{\partial}{\partial r} \left( r \frac{\partial \varphi(r, z)}{\partial r} \right) + \frac{\partial^2 \varphi(r, z)}{\partial z^2} = \frac{qN_d}{\varepsilon_{si}}
\]

where \(\varphi(r, z)\) is the potential distribution in the silicon film, \(N_d\) is the doping in the silicon film, \(q\) is the electron charge and \(\varepsilon_{si}\) is the dielectric permittivity of silicon. The 2D potential distribution \(\varphi(r, z)\) can be obtained using superposition technique. The potential, \(\varphi(r, z)\) can be split into two components: long channel solution \(V(r)\) to the Poisson’s equation and short channel solution \(U(r, z)\) to the Laplace equation i.e.,

\[
\varphi(r, z) = V(r) + U(r, z)
\]
Thus Eq. (1) becomes:
\[
\frac{1}{r} \frac{\partial}{\partial r} \left( r \frac{\partial V(r)}{\partial r} \right) + \frac{\partial^2 V(r)}{\partial r^2} = \frac{q N_f}{\varepsilon_{si}} \tag{2}
\]
\[
\frac{1}{r} \frac{\partial}{\partial r} \left( r \frac{\partial U(r, z)}{\partial r} \right) + \frac{\partial^2 U(r, z)}{\partial r^2} + \frac{\partial^2 U(r, z)}{\partial z^2} = 0 \tag{3}
\]

The boundary conditions required for the solution of 2D potential \( \varphi(r, z) \) are as follows.

The center potential is a function of \( z \) only:
\[
\varphi(r = 0, z) = \varphi_c(z) \tag{4a}
\]

The electric field at the center of the silicon film is zero:
\[
\left. \frac{d\varphi(r, z)}{dr} \right|_{r=0} = 0 \tag{4b}
\]

The electric field at the silicon oxide interface is given by:
\[
\left. \frac{d\varphi(r, z)}{dr} \right|_{r=t_{ao}/2} = \beta \left( V_{gs} - V_{fb} - \varphi \left( r = \frac{t_{ao}}{2}, z \right) \right) \tag{4c}
\]

where
\[
\beta = \frac{C_{oxcyl}}{V_{fb}} \tag{5a}
\]

\( \varphi_c(z) \) is the potential at the center of the silicon film, \( V_{gs} \) is the gate voltage, \( V_{th} \) is the drain voltage, \( V_{fb} \) is the flat band voltage of the oxide, \( t_{ao} \) is the oxide thickness, and \( \varepsilon_{oxcyl} \) is the oxide permittivity.

Now \( V_{fb} \) can be written for three regions as:
\[
V_{fb1} = V_{fb} \quad i = 1, 0 \leq z \leq L_1
\]
\[
V_{fb2} = V_{fb} - \frac{q N_f}{\varepsilon_{oxcyl}} \quad i = 2, L_1 \leq z \leq L_1 + L_2
\]
\[
V_{fb3} = V_{fb} - \frac{q N_f}{\varepsilon_{oxcyl}} \quad i = 3, L_1 + L_2 \leq z \leq L \tag{6}
\]

Here \( N_f \) is the density of localised charges which can be positive or negative. \( V_{fb} \) is the flat band voltage for three different regions as shown in Figure 1. Solution of (2) using boundary conditions (4a)-(4c) can be expressed as:
\[
V_i(r) = \frac{q N_f r^2}{4 \varepsilon_{si}} + V_{gs} - V_{fb} = \frac{q N_f t_{ao}^2}{4 \varepsilon_{si} B_i} - \frac{q N_f t_{ao}^2}{16 \varepsilon_{si}} \tag{7}
\]

The general solution of the Laplace equation in cylindrical coordinates is given by:
\[
U(r, z, \varphi) = \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} J_m(k_m r)(A_{mn} e^{k_m z} + B_{mn} e^{-k_m z})\times (C_{mn} \cos m \phi + D_{mn} \sin m \phi) \tag{8a}
\]

Where \( J_m \) is the Bessel function of order \( m \),\(^{25}\) keeping only terms with \( m = 0 \) (since the potential cannot depend on \( \phi \) due to cylindrical symmetry) we can write it as:
\[
U_i(r, z, \varphi) = \sum_{n=0}^{\infty} J_n(k_n r)(A_{n} e^{k_n z} + B_{n} e^{-k_n z} + C_{n} e^{q N_f t_{ao}^2 (k_n)^2/4})
\]

\[
i = 1, 2, 3 \tag{8b}
\]

Due to rapid decay of the Bessel Fourier series coefficients as shown in Appendix (A8)-(A11) the first term is dominant and the two dimensional potential for the three regions can be expressed as:
\[
\varphi_i(r, z) = \frac{q N_f r^2}{4 \varepsilon_{si}} + V_{gs} - V_{fb} - \frac{q N_f t_{ao}^2}{4 \varepsilon_{si} B_i} + \frac{q N_f t_{ao}^2}{16 \varepsilon_{si}} + J_0(k r)(A_i e^{k_i z} + B_i e^{-k_i z}) \tag{10a}
\]

Where \( A_i \) and \( B_i \) are given in Appendix. Continuous potential for the complete channel length can be written as:
\[
\varphi_i(r, z) = \begin{cases} 
V_{gs} - V_{fb} - \frac{q N_f t_{ao}^2}{4 \varepsilon_{si} B_i} + 2 J_0 \left( \frac{k t_{ao}}{2} \right) \sqrt{A_i B_i} & 0 \leq z \leq L_1 \\
V_{gs} - V_{fb} - \frac{q N_f t_{ao}^2}{4 \varepsilon_{si} B_i} + 2 J_0 \left( \frac{k t_{ao}}{2} \right) \sqrt{A_i B_i} & L_1 \leq z \leq L_1 + L_2 \\
V_{gs} - V_{fb} - \frac{q N_f t_{ao}^2}{4 \varepsilon_{si} B_i} + 2 J_0 \left( \frac{k t_{ao}}{2} \right) \sqrt{A_i B_i} & L_1 + L_2 \leq z \leq L \tag{11a}
\end{cases}
\]

Subthreshold drain current \( I_{sub} \) can be evaluated by using equation of surface potential (10b) as:
\[
I_{sub} = 2 \pi \mu q N_f \int_{V_d}^{V_s} e^{-q \nu_i (z)/kT} dV(z) \tag{12a}
\]

\[
I_{sub} = 2 \pi \mu q N_f \int_{V_d}^{V_s} e^{-q \nu_i (z)/kT} dV(z) \tag{12b}
\]

Here \( V_s \) is the source voltage and \( V_d \) is the drain voltage. From the Subthreshold Current, the threshold Voltage can be calculated using constant current method.\(^{26,27}\) The threshold voltage is measured at the drain current of \( 6 \times 10^{-7} \) A. And subthreshold slope can be expressed as:
\[
S = \left[ \frac{d \log(I_{sub})}{dV_{gs}} \right]^{-1} \tag{13}
\]
3. RESULTS AND DISCUSSION

3.1. Effect on Flat Band Voltage $V_{fb}$

For interface acceptor-type traps which appear at the Si–SiO$_2$ interface, damaged region will accept an electron if the trap level is located beneath the Fermi level. In this situation, damaged region acts as negative localized charge. Similarly a donor type interface trap acts as a positive localised interface charge. Therefore induced interface traps can be transformed into equivalent localised interface charges. The MOS structure of a device form a MOS capacitor, and there is a band bending due to the work function difference between the metal and the semiconductor. The effect of immobile/localised charges at the interface of oxide and semiconductor is such that additional band bending takes place due to these localised charges. Figure 2(a) illustrates that the effect of localised interface charges can be incorporated through change in Flat band Voltage ($V_{fb}$) as the conduction band and valence band energy is raised (lowered) in the damaged region for negative (positive) localised charges. The amount of change in the Flat band voltage ($\Delta V_{fb}$) depends upon the thickness of the gate oxide ($t_{ox}$), permittivity of the oxide ($\varepsilon_{ox}$), and density of interface localised charges ($N_f$) and is given by:28

$$\Delta V_{fb} = \frac{qN_f}{\varepsilon_{ocy}}$$  \hspace{1cm} (14)

Figure 2(b) shows the effect of localised charges on electron concentration. Positive localised charges at the Si–SiO$_2$ interface induces negative charges in the channel thus enhancing the inversion charge density. On the other hand negative localised charges induces positive charges in the channel.

3.2. Effect on Surface Potential and Threshold Voltage

Figures 3(a and b) shows variation in surface potential profile with localised charges. For negative (positive) localised interface charges the surface potential is lowered (increased) in the damaged region because the Flat band voltage ($V_{fb}$) in the damaged region increases (decreases) depending on the nature of localised charges. In case of the negative (positive) interface localised charges, the minimum surface potential appears in the damaged (undamaged) region. Due to the step in the surface potential the damage-free zone is turned on before the damaged one in case of negative localised charges whereas in case of positive localised charges damaged region is turned on first. For $1 \times 10^{16}$ m$^{-2}$ density of localised charges and length of damage region ($= L/2$), threshold voltage is reduced by 11.76% (increased by 26.47% ) in case of positive (negative ) localised charges and this change i.e., $(\Delta V_{th})$ increases as the density of localised charges is increased as shown in Figure 4. The rate of change in threshold voltage $(\Delta V_{th})$ is more for negative localised charges as compared to positive charges because the minimum surface potential remains nearly unchanged for positive localised charges when density of localised charges is increased whereas for negative localised charges minimum surface potential is changed significantly with density of localised charges and its position (i.e., $x_{min}$) shifts more towards the source side as the length of damaged region is increased. Figure 5 shows the impact of length of damaged region on the threshold voltage of the damaged device. When damaged region’s length is small the change in threshold voltage is negligibly small but as the length of damage region increases threshold voltage decreases (increases) for positive (negative) localised charges respectively. Figure 6 shows the effect of varying the radius of silicon pillar on the threshold voltage of undamaged and damaged device. As can be seen from the figure, for
both undamaged and damaged device the threshold voltage increases with decreasing silicon body radius because when the silicon pillar radius is thin the carrier population is confined into the very narrow space where carriers are pushed away from the Si–SiO₂ interface and increases the threshold voltage. Increasing radius of silicon pillar (R) from 5 nm to 15 nm reduces the threshold voltage from 0.258 V to 0.17 V for undamaged device, 0.236 V to 0.15 V for positive localised charges and 0.3 V to 0.216 V for negative localised charges. Figure 7 illustrates the behavior of localised charges located at the source side. When localised charges are induced due to hot carrier effect they are generally located near the drain. But if the localised charges are induced due to radiation damage, plasma etching or stress induced they may occur anywhere at the Si–SiO₂ interface near the source side also. Incident Radiation results in the formation of an electron–hole pair (EHP). The radiation induced electrons are much more mobile than the holes and are swept out of the oxide layer very fast under the influence of strong transverse electric field. The holes that are relatively immobile cause a negative shift of the flat band voltage on the electrical characteristics of device. Thus radiation induced damage generally increases the positive oxide charge density and interface state density which causes device threshold voltage shift and reduce device channel transconductance. Similarly stress induced damage causes charge trapping in the gate oxide and interface states generation at the interface. So when the damaged region is near the drain side and has positive fixed charges, it screens the undamaged region from the drain bias. On the other hand when the damaged region having negative fixed charges is near the source side, undamaged region screens the damaged region. For sub-100 nm device
dimensions, it is increasingly important to model SCEs such as drain-induced barrier lowering (DIBL) and threshold voltage roll-off accurately. Table I shows threshold voltage roll-off due to higher drain bias \( \Delta V_{th} = V_{th} - V_{th0} \) for both damaged and undamaged device. The positive (negative) charges near the drain (source) side effectively suppress the field penetration from the drain, and thus, the threshold voltage reduction due to DIBL is reduced. Therefore, as shown in Table I the reduction in threshold voltage due to higher drain to source voltage \( V_{ds} \) is less in case of positive (negative) localised charges lying near the drain (source) side because of the screening effect. Figure 8 shows threshold voltage reduction (for both undamaged and damaged devices) as the

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**Table I.** Threshold voltage roll-off due to higher drain bias for both damaged and undamaged device. Other parameters are \( L_2 = L/2, L = 70 \text{ nm}, V_{th0} = 0.05 \text{ V}, t_{ox} = 1.5 \text{ nm}, R = 15 \text{ nm}, N_d = 1 \times 10^{26} \text{ m}^{-3}, N_a = 1 \times 10^{21} \text{ m}^{-3}, \varepsilon_s = 3.9. \)

<table>
<thead>
<tr>
<th>( L_2 )</th>
<th>( L_1 )</th>
<th>( N_d )</th>
<th>( V_{th0} )</th>
<th>( V_{th0} )</th>
<th>( V_{th0} )</th>
<th>( \Delta V_{th} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>170</td>
<td>156</td>
<td>14</td>
<td>164</td>
</tr>
<tr>
<td>35</td>
<td>0</td>
<td>( 10^{16} )</td>
<td>150</td>
<td>132</td>
<td>18</td>
<td>134</td>
</tr>
<tr>
<td>35</td>
<td>35</td>
<td>( 10^{16} )</td>
<td>134</td>
<td>106</td>
<td>28</td>
<td>130</td>
</tr>
<tr>
<td>35</td>
<td>0</td>
<td>( -10^{16} )</td>
<td>215</td>
<td>190</td>
<td>25</td>
<td>197</td>
</tr>
<tr>
<td>35</td>
<td>35</td>
<td>( -10^{16} )</td>
<td>222</td>
<td>210</td>
<td>12</td>
<td>198</td>
</tr>
</tbody>
</table>

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**Fig. 6.** Threshold voltage as a function of density of localised charges. Other parameters are: \( L_1 = 35 \text{ nm}, V_{th0} = 0.05 \text{ V}, L = 70 \text{ nm}, t_{ox} = 1.5 \text{ nm}, R = 15 \text{ nm}, N_d = 1 \times 10^{26} \text{ m}^{-3}, N_a = 1 \times 10^{21} \text{ m}^{-3}. \)

**Fig. 7.** Surface potential along the channel when damaged region is located near the source side. Other parameters are \( V_{th0} = 0 \text{ V}, V_{th0} = 0 \text{ V}, L = 70 \text{ nm}, t_{ox} = 1.5 \text{ nm}, R = 15 \text{ nm}, N_d = 1 \times 10^{26} \text{ m}^{-3}, N_a = 1 \times 10^{21} \text{ m}^{-3}. \)

**Fig. 8.** Threshold voltage as a function of channel length. Other parameters are: \( L_2 = L/2, V_{th0} = 0.05 \text{ V}, t_{ox} = 1.5 \text{ nm}, R = 15 \text{ nm}, N_d = 1 \times 10^{26} \text{ m}^{-3}, N_a = 1 \times 10^{21} \text{ m}^{-3}. \)

**Fig. 9.** Subthreshold current as a function of Gate to Source Voltage. Other parameters are \( L_2 = 35 \text{ nm}, L = 70 \text{ nm}, t_{ox} = 1.5 \text{ nm}, R = 15 \text{ nm}, N_d = 1 \times 10^{26} \text{ m}^{-3}, N_a = 1 \times 10^{21} \text{ m}^{-3}. \)
channel length decreases. The decrease in channel length reduces gate controlled channel charge thereby decreasing the threshold voltage. When channel length is reduced from 77 nm to 45 nm threshold voltage is reduced by 40 mV (50 mV) in case of positive (negative) localised charges.

### 3.3. Effect on Subthreshold Current and Subthreshold Slope

Change in the charge distribution, flat band voltage, potential and threshold voltage due to localised charges leads to degradation of subthreshold current and subthreshold slope. Positive (negative) localised charges result in the increase (decrease) of subthreshold current as shown in Figure 9. For negative localised charges $I_{on}$ ($I_{off}$) decreases by 0.9 $\mu$A (1.01 nA) whereas for positive localised charges $I_{on}$ ($I_{off}$) increases by 0.7 $\mu$A (2.48 nA). Thus Positive localised charges increases both the $I_{on}$ and $I_{off}$ but the order of the increase in the $I_{off}$ is much more than the $I_{on}$. The overall result is that the $I_{on}/I_{off}$ ratio is reduced from $1.9 \times 10^4$ to $6.8 \times 10^3$ for positive localised charges and increased from $1.9 \times 10^4$ to $9.1 \times 10^4$ for negative localised charges. Figure 10 shows that subthreshold slope variation with channel length for both damaged and damage-free device. Subthreshold slope is more (less) in case of positive (negative) localised charges because of the enhancement (decrease) in the subthreshold current (i.e., off-current). At 70 nm gate length positive (negative) localised charges increases (decreases) the subthreshold slope by 1.56% (1.06%). Figure 11 shows the effect of radius of silicon pillar on the subthreshold current for both undamaged and damaged device. As is clear from the figure thicker silicon body leads to higher $I_{off}$. For undamaged device increasing silicon pillar radius ($R$) from 5 nm to 15 nm increases the $I_{off}$ from 0.061 nA to 1.27 nA. Similarly for positive localised charges $I_{off}$ increases from 0.124 nA to 3.75 nA and for negative localised charges $I_{off}$ increases from 0.012 nA to 0.26 nA. However, regardless of higher subthreshold leakage, thicker silicon bodies...
provide higher driving current which is proportional to area $\pi t_h^2$. Thus for applications where low off current is required device with smaller value of $R$ should be used. The trade-off between how to keep low subthreshold degradation and to have high driving capability should be accounted for simultaneously as the device is designed for the circuit application.

4. CONCLUSION

Presence of Localised charges at Si–SiO₂ interface causes a step in the potential profile which results in the shift of threshold voltage, degradation of subthreshold current and subthreshold slope of the device. The analytical results are verified with the simulated results and it can be concluded from the results that negative (positive) localised charges leads to increase (decrease) in threshold voltage and decrease (increase) in subthreshold current and subthreshold slope of the device.

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APPENDIX

The continuity of surface potential and electric field must satisfy at interfaces of damaged and damage free regions, i.e.,

$$\psi_i(r, L_1) = \psi_2(r, L_1) \quad \text{(A1-a)}$$

$$\psi_i(r, L_1 + L_2) = \psi_2(r, L_1 + L_2) \quad \text{(A1-b)}$$

$$\psi_i'(r, L_1) = \psi_2'(r, L_1) \quad \text{(A1-c)}$$

$$\psi_i'(r, L_1 + L_2) = \psi_2'(r, L_1 + L_2) \quad \text{(A1-d)}$$

and the boundary conditions at the source and drain edges are

$$\psi_i(r, 0) = V_{bi} \quad \text{(A1-e)}$$

$$\psi_3(r, L) = V_{bi} + V_{ds} \quad \text{(A1-f)}$$

where $V_{bi}$ is the built-in potential of the source/drain junction. Applying these conditions in (10a), we can solve to obtain:

$$\phi_i = V_{bi} - V_{bi} - \frac{qN_d l_t_i}{4\epsilon_R \beta} = \frac{qN_d r_i^2}{16\epsilon_R} \quad \text{(A2)}$$

$$X = \frac{R^2 J_s^2(kR)}{2} + \frac{R^2 J_s^2(kR)}{2} \quad \text{(A3)}$$

$$P = \frac{\phi_i R_j(kR)}{kX} + \frac{(qN_d / \epsilon_R)(kR^3 J_s(kR) + 2R^2 J_s(kR))}{4k^2 X} \quad \text{(A4)}$$

$$Q = \frac{\phi_i R_j(kR)}{kX} + \frac{(qN_d / \epsilon_R)(kR^3 J_s(kR) + 2R^2 J_s(kR))}{4k^2 X} \quad \text{(A5)}$$

$$A_2 = \frac{b_1 b_2 - b_2 b_3}{b_1 c_2 - b_2 c_2} \quad \text{(A6)}$$

$$B_2 = \frac{b_1 b_2 - b_2 b_3}{b_1 c_2 - b_2 c_2} \quad \text{(A7)}$$

$$A_1 = \frac{(V_{bi}(R_j(kR)/kX) - P)e^{-kL_1} + A_3 e^{kL_1} - B_1 e^{-kL_1}}{2 \cosh(kL_1)} \quad \text{(A8)}$$

$$B_1 = \frac{(V_{bi}(R_j(kR)/kX) - P)e^{kL_1} - A_2 e^{kL_1} + B_2 e^{-kL_1}}{2 \cosh(kL_1)} \quad \text{(A9)}$$

$$A_1 = (((V_{bi} + V_{ds})R_j(kR)/kX - P)e^{-k(L_1 + L_2)} + (A_2 e^{kL_1}) - B_2 e^{-k(L_1 + L_2)}) \cdot (2 \cosh(kL_3))^{-1} \quad \text{(A10)}$$

$$B_1 = (((V_{bi} + V_{ds})R_j(kR)/kX - P)e^{kL_1} - (A_2 e^{kL_1}) - B_2 e^{-k(L_1 + L_2)}) \cdot (2 \cosh(kL_3))^{-1} \quad \text{(A11)}$$

Where

$$b_1 = (1 - \tanh kL_1) \cdot e^{kL_1} \quad \text{(A12)}$$

$$b_2 = (1 + \tanh kL_1) \cdot e^{-kL_1} \quad \text{(A13)}$$

$$b_3 = P - Q + \frac{V_{bi}(R_j(kR)/kX) - P}{\cosh kL_1} \quad \text{(A14)}$$

$$b_3 = (1 + \tanh kL_3) \cdot e^{kL_1} \quad \text{(A15)}$$

$$b_3 = (1 - \tanh kL_3) \cdot e^{-kL_1} \quad \text{(A16)}$$

$$b_6 = P - Q + \frac{V_{bi}(R_j(kR)/kX) - P}{\cosh kL_3} \quad \text{(A17)}$$

References


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