Effect of localised charges on nanoscale cylindrical surrounding gate MOSFET: Analog performance and linearity analysis

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A R T I C L E   I N F O

Article history:
Received 26 April 2011
Received in revised form 8 December 2011
Accepted 8 December 2011
Available online 4 January 2012

A B S T R A C T

The paper presents a simulation study of Nanoscale Cylindrical Surrounding Gate (SRG) MOSFET with localised interface charges. The objective of the present work is to study the performance degradation due to hot carrier induced/radiation induced/stress induced damage in the form of localised/ixed charges at the semiconductor/oxide interface of the device. Impact of fixed charges has been studied on the characteristics such as drain current, transconductance and its higher order terms, device efficiency and linearity FOMs. Effect of nature and extension of interface fixed charges has been discussed in detail through extensive simulation. Circuit reliability issues of the device are discussed in terms of DC bias point degradation.

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1. Introduction

The explosive growth of communication technology has created mass consumer market for Radio-Frequency (RF) electronics. Mobile communications as an example is one of the fastest growing areas over the past decade and semiconductor devices for RF applications are the backbone of advanced communication systems. In addition to digital circuits, MOSFET remain a strong contender for analog RF applications in the wireless communications market [1–3]. As a result, RF performance of CMOS devices has attracted significant amount of interest [4–6]. Majority of these RF CMOS studies however, place the emphasis only on understanding of several RF figures of merit (FOMs) such as cut-off-frequency, maximum oscillation frequency, noise figure and gm/Id characteristics which are important for analog design. But to reveal the linearity performance of devices, another important FOM called Linearity in RF design is used. Kang et al. [5] reported the linearity analysis of bulk CMOS based on compact device model. Non-linearity in a device is manifested by the presence of higher-order ‘harmonics’ at the output signal. Linearity ensures that higher order harmonics and inter-modulation terms are negligible. Adan et al. [7] reported experimental RF performance of SOI MOSFET including linearity study of single gate SOI MOSFET. There are several papers reported on analog and RF performance of SOI MOSFET [8–11] and DG MOSFET [12–14]. Surrounding Gate (SRG) MOSFET is one of the most promising device structure to extend the scaling of the CMOS device as it provides the best electrostatic control of the channel which further improves with the reduction of the gate length and gate oxide thickness [15–18]. Research work related to analog and RF performance of SRG MOSFET has been reported previously [19,20] indicating that SRG MOSFET exhibit superior intrinsic RF scaling capability and are suitable for low-power analog/RF applications.

Apart from short channel immunity, long term reliability is a major concern for nanoscale devices. Device performance degradation due to interface traps induced at the Si–SiO2 interface raises serious device reliability issues. These interface traps are induced due to: (1) process induced damage [21], (2) stress induced damage [22], (3) radiation induced damage [23] and (4) hot carrier induced damage [24]. For interface acceptor-type traps which appear at the Si–SiO2 interface, damaged region will accept an electron if the trap level is located beneath the Fermi level. In this situation, damaged region acts as negative fixed charge. Similarly, a donor type interface trap acts as a positive localised interface charge. Therefore induced interface traps can be treated as effective localised interface charges. A lot of research work has been done to study the effect of localised charges [25–28] on electrical performance of the SRG MOSFET in terms of surface potential and threshold voltage.

In this paper the impact of localised charges on analog and linearity performance of Nanoscale Cylindrical Surrounding Gate (SRG) MOSFET has been studied. For this purpose, a uniform distribution for the interface charge density has been employed in the damaged region which makes the analysis simple enough to understand the reasons for the performance degradation. Further the impact of density, polarity, extension and position of the
Localised charges on the electrical characteristics of the device is studied extensively through device simulation.

2. Linearity analysis

To model the non-linearity in a MOSFET (modulated with an AC gate voltage) drain current $I_{ds}$ can be viewed as a time variant non-linear system:[5]

$$I_{ds} = I_0 + g_{m1}V_{gs} + g_{m2}V_{gs}^2 + g_{m3}V_{gs}^3 + \cdots$$

where Taylor expansion coefficients $g_{mn}$ are

$$g_{mn} = \frac{\partial^n I_{ds}}{\partial V_{gs}^n} : n = 1, 2, 3$$

and $I_0$ is the current at DC operation point. $g_{mn}$ represents the n-th order derivative of $I_{ds}$ with respect to $V_{gs}$.

Non-linear behaviour of MOSFET results in wasting useful output power. Moreover, the third-order non-linearity term, $g_{m3}$ is especially troublesome for RF systems, since it leads to intermodulation. The performance matrices used in this work to evaluate the device linearity performance are transconductance and its higher order coefficients ($g_{m1}$, $g_{m2}$ and $g_{m3}$) to determine the optimum DC bias point, the device Figures of merit: $VIP_2$ (Second Order Voltage Intercept Point), $VIP_3$ (Third Order Voltage Intercept Point) and $IIP_3$ (Third-Order Input Intercept Point) [1],[18]. $VIP_2$, $VIP_3$, and $IIP_3$ are defined as [1,5]:

$$VIP_2 = \frac{4g_{m1}g_{m2}}{3}$$

$$VIP_3 = \sqrt{\frac{24g_{m1}}{g_{m3}}}$$

$$IIP_3 = \frac{2g_{m1}}{3g_{m3}R_s}$$

where $R_s = 50\ \Omega$ for most RF applications.

3. Calibration and simulation section

Nanoscale Surrounding Gate (SRG) MOSFET with interface localised charges has been simulated using ATLAS-3D device simulator [29] and the schematic cross section of the structure with interface fixed charges is shown in Fig. 1. CVT mobility model with parameters (for electrons $\alpha_{fn} = 0.68$, $\beta_{fn} = 2$, $\gamma_{fn} = 2.5$, $\nu_{sat} = 1.03 \times 10^7 \text{cm/s}$, $\mu_{on} = 52.2 \text{cm}^2/\text{V s}$, $\mu_{max} = 1417 \text{cm}^2/\text{V s}$ and for holes $\alpha_{ph} = 0.71$, $\beta_{ph} = 2$, $\gamma_{ph} = 2.2$, $\nu_{sat} = 0.3 \times 10^7 \text{cm/s}$, $\mu_{op} = 44.9 \text{cm}^2/\text{V s}$, $\mu_{max} = 470.5 \text{cm}^2/\text{V s}$) is used to calibrate simulation results with experimental results [31]. CVT model considers parallel and perpendicular field dependence of mobility and mobility reduction effects due to various scattering mechanisms. The electron and hole saturation velocities used in the simulation are $1.03 \times 10^7 \text{cm/s}$ and $0.3 \times 10^7 \text{cm/s}$ [32] respectively. SRH recombination model with carrier lifetime ($1 \times 10^7$ s) was used to account for minority recombination. Bohr quantum potential model with parameters ($\alpha = 0.3$, $\gamma = 0.01$) was used to take QMEs (Quantum Mechanical Effects) into consideration. Energy relaxation
time of 0.4 ps was used in the Energy Balance Transport (EBT) model to account for non-local transport effects such as velocity overshoot, diffusion associated with the carrier temperature and the dependence of impact ionisation rates on carrier energy distributions. All these phenomena have a significant effect on the terminal properties of nanoscale devices as reported in [30,33]. Close proximity of simulated results (after calibration) to $I_{DS}$ vs $V_{GS}$ and $I_{DS}$ vs $V_{DS}$ with experimental results as shown in Fig. 2 validate the choice of model parameters used in the simulation.

The damaged region of length $L_d$, which is present at the Si–SiO$_2$ interface is simulated in ATLAS using position parameters of the INTERFACE statement. The extension and location of damaged region can be in the direction along the channel having distance from drain as $L_d$ so that damage free part is $L_1 = L - L_2 - L_3$. Density of fixed charges has been set using the QF parameter in the INTERFACE statement. The extension and location of damaged region can be in the direction along the channel using XMIN and X.MAX position parameters of the INTERFACE statement. For cylindrical structures $Z$ coordinate is used in place of $X$ to represent the direction along the channel. Fig. 3 shows the potential contour plot for $L_1 = 12$ nm, $L_2 = 16$ nm and $L_3 = 4$ nm. Here localised charges are present only in the region from $L_1$ to $L_1 + L_2$ whereas QF is 0 in the regions 0 to $L_1$ and $L_1 + L_2$ to $L$. In this analysis most of the results are plotted for the case when localised charges are present over half of the Si/SiO$_2$ interface near the drain side (i.e. $L_1 = L_2 = L/2$, $L_3 = 0$) as the drain end is more prone to the damage because of the high field. However the impact of variation in the extension and position of localised charges has also been studied on the device performance.

4. Result and discussion

There are various mechanisms which cause damage to the device like stress induced damage [21,22] which can be of two types: electrical stress and process damage i.e. induced by plasma etching. The need for submicron devices in today’s CMOS circuitry necessitates the use of plasma etching for pattern transfer processes [22]. However, the damage to the gate oxide and oxide/Si interface induced by plasma etching can adversely affect MOSFETs manufacturing yield, performance and reliability. For MOS technologies, ionising radiation [23] generally increases the positive oxide charge density and interface state density which can cause shift in the threshold voltage and reduces transconductance of the device. Incident radiation results in formation of an electron–hole pair (EHP) and since the electrons are much more mobile than the holes, they are swept out of the oxide layer very fast under the influence of strong transverse electric field. The holes that are relatively immobile result in a negative shift of the flat band voltage in the electrical characteristics of device. The degradation of MOSFET characteristics due to the injection of hot carriers [24] into the gate oxide stands as one of the most important challenges for device scaling. The hot-carrier effect is mainly caused by the high electric field in the channel near the drain junction which provides enough energy to the channel electrons which may generate EHPs through impact ionisation. The holes which are generated forms the substrate current and the electrons are swept towards the drain. In case electrons get enough energy (i.e. to reach the Si–SiO$_2$ interface) and surmount the barrier, gate current increases which leads to interface traps and localised interface charges near the drain junction. Localised charges at the Si–SiO$_2$ interface causes additional bending under the gate which in turn causes change in flat band voltage in the damaged region. The amount of change in the flat band voltage ($\Delta V_{FB}$) depends upon the thickness of the oxide ($t_{ox}$), permittivity of the oxide ($\epsilon_{ox}$), and density of interface fixed charges ($N_f$) and is given by [34]:

![Fig. 4. Impact of Localised charges on the transfer characteristics. Hollow symbols: positive Localised charges and solid: negative Localised charges. Other parameters are $L = 32$ nm, $L_2 = 16$ nm, $L_3 = 0$, $t_{ox} = 1.5$ nm, $R = 5$ nm, $N_d = 1 \times 10^{26}$ m$^{-3}$, $N_a = 1 \times 10^{21}$ m$^{-3}$, $V_{DS} = 0.05$ V.](image)

![Fig. 5. Transconductance as a function of Gate to Source Voltage for various values of localised charge density. Other parameters are $L = 32$ nm, $L_2 = 16$ nm, $L_3 = 0$, $t_{ox} = 1.5$ nm, $R = 5$ nm, $N_d = 1 \times 10^{26}$ m$^{-3}$, $N_a = 1 \times 10^{21}$ m$^{-3}$, $V_{DS} = 0.05$ V.](image)

![Fig. 6. Transconductance as a function of Gate to Source Voltage for various values of silicon pillar radius. Other parameters are $L = 32$ nm, $L_2 = 16$ nm, $L_3 = 0$, $t_{ox} = 1.5$ nm, $N_d = 1 \times 10^{26}$ m$^{-3}$, $N_a = 1 \times 10^{21}$ m$^{-3}$, $V_{DS} = 0.05$ V.](image)

![Fig. 7. Transconductance as a function of Gate to Source Voltage for two different channel lengths. Other parameters are $L = 1/2$, $L_3 = 0$, $t_{ox} = 1.5$ nm, $N_d = 1 \times 10^{20}$ m$^{-3}$, $N_a = 1 \times 10^{19}$ m$^{-3}$, $V_{DS} = 0.05$ V.](image)
$\Delta V_{fb} = \frac{qN_f}{C_{asyf}}$  \hspace{1cm} (6)

where $C_{asyf}$ is the gate oxide capacitance per unit area of the cylindrical-gate MOSFET, and is given as:

$$C_{asyf} = \frac{2\varepsilon_{ox}}{t_{ox} \ln \left(1 + \left(\frac{L}{t_{ox}}\right)^2\right)}$$  \hspace{1cm} (7)

### 4.1 Analog performance

When localised charges are present over half of the interface near the drain side (i.e. $L_1 = L_2 = L/2$, $L_3 = 0$), change in flat band voltage causes surface potential to be lowered (raised) in case of negative (positive) localised charges in the damaged region w.r.t. the undamaged region. Thus, localised charges give rise to change in the minimum surface potential and its position and induces a shift in the threshold voltage. When half of the channel region is damaged (near the drain side) and density of positive (negative) localised charges is $1 \times 10^{16}$ m$^{-2}$, the threshold voltage is reduced by 8.3% (increased by 20.47%). Positive fixed charges give rise to enhanced drain current whereas negative fixed charges lead to decrease in drain current as shown in Fig. 4. As can be seen from Fig. 4, the order of change is greater in case of negative charges as compared to positive charges and the change increases with the intensity of localised charges. This is because minimum surface potential and its position remains nearly unchanged for positive fixed charges whereas it changes significantly in case of negative fixed charges. Drain current degradation due to localised charges leads to transconductance degradation. Fig. 5 shows that fixed charges cause degradation of transconductance of the device. Positive (negative) fixed charges cause increase (decrease) in transconductance in subthreshold region. At $V_{gs} = 0.2$ V, transconductance is enhanced (reduced) by 33% (61.2%) for damaged device with positive (negative) localised charges w.r.t. the undamaged device. However in case of strong inversion region transconductance is higher for negative fixed charges. At $V_{gs} = 0.5$ V transconductance is increased by 10.16% (19.4%) for damaged device with positive (negative) localised charges w.r.t. the undamaged device. The degradation caused by localised charges is more in subthreshold and linear region than in saturation region because for $V_{gs} \gg V_{th}$, gate bias has lesser influence on band bending and the surface potential is also pinned.

The peak value of transconductance ($g_{m}$) decides the DC bias point for optimum device operation. Higher gain can be achieved by setting DC bias close to $V_{gs_{opt}} = V_{gs_{max}}$. This optimum bias point, shifts towards lower (higher) gate to source voltage ($V_{gs}$) for positive (negative) fixed charges w.r.t. the undamaged device. This change in optimum bias point is due to change in threshold voltage and drain current induced by the localised charges. As shown in Fig. 5 optimum bias point is shifted by 7.6% (30.7%) for positive (negative) localised charges for $N_f = 1 \times 10^{16}$ m$^{-2}$ and increases to 11.5% (46.15%) when density of positive (negative) localised charges is doubled. The change in the peak $g_{m}$ value depends upon the change in the minimum surface potential value and shift in the bias point (i.e. $V_{gs}$ corresponding to peak $g_{m}$) depends on the shift in the position of minimum surface potential and both are functions of density of localised charges. For $N_f = 1 \times 10^{16}$ m$^{-2}$ the change in peak $g_{m}$ value is very small (i.e. equal to $qN_f/ C_{ox} = 0.06$ V) but Fig. 5 shows that peak value of $g_{m}$ (i.e. $g_{m_{max}}$) increases as the density of localised charges ($N_f$) increases. The change in bias point is greater for negative localised charges because when localised charges are present over half of the interface (i.e. $L_1 = L_2 = L/2$) near the drain side (i.e. $L_3 = 0$), the minimum surface potential appears in the damaged (undamaged) region for negative (positive) localised charges. This implies that in case of negative localised charges, there is large change in minimum surface potential value in comparison to the case when positive localised charges are present, resulting in a greater $V_{th}$ shift. Thus when localised charges are present over the whole interface, shift in the threshold voltage and bias point is same for both positive and negative localised charges because in both case change in minimum surface potential is same.

Fig. 6 illustrates the effect of silicon pillar radius on the transconductance for both undamaged and damaged device. For enhanced current driving capability and higher device gain, radius of silicon body should be large but it leads to poor short channel...
immunity and off current degradation. When radius ($R$) is increased from 5 nm to 15 nm it leads to 79%, 77% (78%) enhancement in transconductance value for undamaged device, damaged device with positive (negative) localised charges. But the off current increases from $6.7 \times 10^{-3}$ $\mu A/\mu m$ to $7.2 \times 10^{-1}$ $\mu A/\mu m$ for undamaged device, $1.73 \times 10^{-2}$ $\mu A/\mu m$ to $1.59 \mu A/\mu m$ for damaged device with positive localised charges and $1.45 \times 10^{-3} $ $\mu A/\mu m$ to $3.07 \times 10^{-1}$ $\mu A/\mu m$ for negative localised charges. Thus thicker silicon body leads to higher current driving capability but at the same time it results in higher leakage current. Also at $R = 15$ nm, the change in $g_m$ caused due to localised charges is two times less than that at $R = 5$ nm for both positive and negative localised charges. Fig. 7 shows the impact of reducing the channel length on the transconductance. As channel length reduces from 70 nm to 32 nm, there is an improvement of 23.7%, 24.8% and 21.8% in peak value of transconductance ($g_m$) for undamaged, positive fixed charges and negative fixed charges respectively.

Device efficiency ($g_m/I_{ds}$) is also an important parameter as higher $g_m/I_{ds}$ values indicate higher transconductance and thus stronger capability to convert dc power into ac gain performance. For analog applications, shift in the bias region of operation as compared to saturation region thus localised charges also lead to shifting in the zero crossover point (ZCP) which is another parameter which decides DC bias point for optimum device operation and hence the non-linear behaviour of $g_m$ can be minimised by setting DC bias close to Zero Crossover Point (ZCP). Localised charges also lead to shifting in the zero crossover point as shown in Fig. 10. For positive (negative) localised charges, zero crossover point shifts towards lower (higher) gate voltage. An amplifier maintains a constant gain for low level input signals. However at higher input levels, the amplifier goes into saturation and its gain decreases. The non-linearity exhibited by higher order derivatives of $I_{ds} - V_{gs}$ characteristics (generally $g_m$), determines a lower limit on the distortion and hence the amplitude of $g_m$ and $I_{ds}$ should be minimum for better linear performance. Fig. 10 shows the variation of higher order derivatives of $I_{ds} - V_{gs}$ with $V_{gs}$. It shows that at higher $V_{gs}$ values (i.e. strong inversion region) $g_m$ is lower (higher) for positive (negative) fixed charges w.r.t. the undamaged device. The zero crossover point (ZCP) (i.e. $V_{gs}$ value at which $g_m$ become zero) is another parameter which decides DC bias point for optimum device operation and hence the non-linear behaviour of $g_m$ can be minimised by setting DC bias close to Zero Crossover Point (ZCP). Localised charges also lead to shifting in the zero crossover point as shown in Fig. 10. For positive (negative) localised charges, zero crossover point shifts towards lower (higher) gate voltage. An amplifier maintains a constant gain for low level input signals. However at higher input levels, the amplifier goes into saturation and its gain decreases. The 1-dB compression point indicates the power level that causes the gain to drop by 1-dB from the Fig. 9, transconductance is higher and drain conductance is lesser for negative localised charges thus giving higher intrinsic voltage gain ($g_m(V_{ds})$). The impact of localised charges on $g_m$, $g_m/I_{ds}$, $g_m/g_d$ and $g_m/g_d$ is much more prominent in subthreshold and linear region of operation as compared to saturation region thus localised charges play a detrimental role for device when used for switching applications. Similarly, for analog applications, shift in the bias point and zero crossover point is a serious issue.

4.2. Linearity performance

Fig. 11. Comparison of 1-dB compression point for undamaged and damaged device. Other parameters are $L = 32$ nm, $L_2 = 16$ nm, $L_3 = 0$, $t_{ox} = 1.5$ nm, $R = 5$ nm, $N_f = 1 \times 10^{26}$ m$^{-3}$, $N_d = 1 \times 10^{21}$ m$^{-3}$, $V_{ds} = 0.05$ V.

Fig. 12. VIP2 as a function of Gate to Source Voltage. Other parameters are $L = 32$ nm, $L_2 = 16$ nm, $L_3 = 0$, $t_{ox} = 1.5$ nm, $R = 5$ nm, $N_f = 1 \times 10^{26}$ m$^{-3}$, $N_d = 1 \times 10^{21}$ m$^{-3}$, $V_{ds} = 0.05$ V.

Fig. 13. VIP3 as a function of Gate to Source Voltage. Other parameters are $L = 32$ nm, $L_2 = 16$ nm, $L_3 = 0$, $t_{ox} = 1.5$ nm, $R = 5$ nm, $N_f = 1 \times 10^{26}$ m$^{-3}$, $N_d = 1 \times 10^{21}$ m$^{-3}$, $V_{ds} = 0.05$ V.

Fig. 14. VIP3 as a function of Gate to Source Voltage. Other parameters are $L = 32$ nm, $L_2 = 16$ nm, $t_{ox} = 1.5$ nm, $R = 5$ nm, $N_f = 1 \times 10^{26}$ m$^{-3}$, $N_d = 1 \times 10^{21}$ m$^{-3}$, $V_{ds} = 0.05$ V.
its small signal value. The 1-dB compression point can, thus, be considered as a measure of the onset of distortion and is given by:

\[
1 \text{dB Compression point} = 0.22 \sqrt{\frac{g_m}{g_{m3}}}
\]  

(8)

Fig. 11 shows the impact of localised charges on 1 dB compression point. As shown in Fig. 11 damaged device with positive (negative) localised charges exhibits higher 1-dB compression point as compared to undamaged device.

For any system to act linearly it should stay below the 1-dB compression point [1]. Linearity is one of RF figures of merit and has applications for gain and noise. For better linearity performance VIP2, VIP3, IIP3 should be as high as possible. Figs. 12–14 clearly show that peak value of VIP2, VIP3, and IIP3 increases (decreases) in presence of positive (negative) fixed charges as compared to the undamaged device in both subthreshold and inversion regions. Also the position of peak value of these figures of merit (FOM) shifts towards lower (higher) in inversion regions. Also the position of peak value of these figures compared to the undamaged device in both subthreshold and linear region.

5. Conclusion

Effect of localised charges has been studied on transconductance and its higher derivatives, optimum bias point, zero crossover point, device efficiency, linearity figures of merit and 1 dB compression point of nanoscale cylindrical SRG MOSFET through extensive simulations. The important conclusion drawn from the results is that localised charges present at the Si–SiO2 interface causes a shift in the flat band voltage and hence results in the shift of threshold voltage, degradation of drain current, transconduction, device gain, device efficiency and linearity performance. The parameters for amplifier design like g_m, g_m/ide, E_D and g_m/β are more degraded in subthreshold and linear region as compared to saturation region. As in most conventional amplifiers, MOSFET is operated in saturation region or in linear region, therefore the overall performance degradation of the amplifier caused due to localised charges will be small. Therefore presence of localised charges is more hazardous when device is to be operated in subthreshold region (i.e. switching applications) because of higher degradation in subthreshold region. Another serious implication is the shifting in the bias point which can be harmful for circuit reliability. Since these localised charges are always present in a practical device, this study of estimation of performance degradation as a function of density, polarity, extension and position of localised charges is essential so that device can be optimised accordingly.

Acknowledgement

Author (Rajni Gautam) is thankful to University Grants Commission (UGC), Government of India for necessary financial assistance to carry out this research work.

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