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Two-dimensional analytical sub-threshold model of multi-layered gate dielectric recessed channel (MLaG-RC) nanoscale MOSFET

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Abstract

In this paper, for the first time, a two-dimensional (2D) analytical sub-threshold model for sub-50 nm multi-layered gate dielectric recessed channel (MLaG-RC) MOSFET is presented and investigated using an ATLAS-2D device simulator, to counteract the large gate leakages and increased standby power consumption that arise due to continued scaling of SiO₂-based gate dielectrics. The 2D model has been developed using a cubic polynomial potential distribution approach and includes the evaluation of surface potential, electric field along the channel, threshold voltage, drain-induced barrier lowering (DIBL), sub-threshold drain current and sub-threshold swing using the minimum surface potential. A good agreement between the model predictions and device simulation results is obtained, verifying the accuracy of the proposed analytical model.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

The steady downscaling of device dimensions over the past few decades has been the main stimulus in the growth of integrated circuits and information industry. The pervasiveness of silicon-based ICs in electronic systems continues as the industry moves into the ultra-large-scale integration (ULSI) age. As the MOSFET dimensions scale down to the sub-50 nm regime, further scaling down of SiO₂ gate dielectric leads to high direct tunneling gate leakage current, which in turn causes increase in device power consumption. This critical issue necessitates the introduction of high-K materials for Sub-50 nm technology node so that the physical thickness of the oxide layer \( t_{ox} = t_{ox1} + t_{ox2} \) increases, keeping the effective oxide thickness (EOT) same. High-K dielectrics have lower leakage current than SiO₂ for the same EOT, because of the larger physical thickness of high-K dielectric. Increasing physical gate dielectric thickness, however, results in a higher gate-fringing field that reduces the gate control and aggravates short channel effects (SCEs) [1–7]. Thus, an ultra thin SiO₂ interlayer between the high-K layer and silicon substrate was introduced (resulting in a multi-layer gate structure) to improve the interface quality and stability. The CMOS transistors designed with multi-layer high-K gate dielectrics achieve the expected high drive current performance and lower leakage current, thereby proving its efficacy for high performance CMOS logic applications. The metal gate/high-K dielectric and SiO₂ multi-layered gate architecture exhibit negligible gate oxide leakage and channel mobilities close to SiO₂ [4, 7]. Further, to achieve higher speeds and higher packing densities, gate length miniaturization is the key parameter, but it leads to SCEs and hot carrier effects. Recessed channel (RC) MOSFET [8–12] structures are considered as potential candidates to suppress and overcome SCEs, punch-through and DIBL even...
at gate lengths down to the sub-50 nm regime because negative junctions can be fabricated without any increase in the series resistance and hence, for use in CMOS ULSI circuits. MLaG-RC MOSFET design, considered in this study integrates the desired features of multi-layered gate architecture [4–6] such as improvement in gate controllability and reduction in gate leakage and tunneling effects; and those allied with RC MOSFET [8–12] such as excellent hot carrier immunity, SCE and punchthrough suppression, thereby enhancing the gate controllability over the channel and the electrical and switching characteristics in terms of DIBL, subthreshold swing and hot carrier effects. Thus, multi-layered dielectric gate architecture in conjunction with recessed channel structure is of paramount importance in nanoscale devices. Although the proposed MLaG-RC structure has not yet been fabricated, recessed channel MOSFET and multi-layered gate structures (i.e. gate oxide stack) have already been fabricated; and thus, the fabrication feasibility of such a structure (i.e. MLaG-RC) seems possible due to various integration schemes reported in the literature. For the feasibility of the recessed channel MOSFET structure, several integration schemes have been suggested such as plasma etching and LOCOS isolation [8], reactive ion etching and LOCOS isolation technique [9], self-aligned CMP, where, the self-aligned process was defined by the groove etching and polysilicon CMP steps [13], and shallow trench isolation (STI) where gate oxide films were produced with a conventional furnace and the oxide films for gate electrode was deposited by LP CVD at 850°C [14]. Moreover, in addition to this, fabrication schemes are also available for high-K gate stack architectures such as reactive sputtering and oxidation [15]; atomic layer deposition technique [16] and plasma nitridation coupled with metal–organic chemical vapor deposition (MOCVD) [17]. Nevertheless, history has shown that what is only theoretical, and practically unfeasible when first proposed, may well become practical and even useful as technology advances.

Nobel Laureate Professor Herb Kroemer has pointed out that his initial ideas on the HBT were not able to be realized in devices until more than two decades with the emergence of MBE. The MLaG-RC MOSFET (figure 1), is thus proposed with an optimistic outlook.

To gain insight into the effectiveness of MLaG-RC MOSFET design, a simple 2D analytical model has been developed by solving the 2D Poisson equation and the modeled results are validated using the ATLAS-2D device simulation [18] results. Standard TCAD tools can be set up very easily to analyze the structures. However, in order to optimize the operation of the proposed structure, an accurate understanding of the physical behavior and physical phenomena occurring in the device is a must. Two-dimensional (2D) analytical model enables a systematic, fast, physics-based analysis of MOSFET design, a simple 2D analytical model has been developed by solving the 2D Poisson equation and the modeled results are validated using the ATLAS-2D device simulator [18]. Standard TCAD tools can be set up very easily to analyze the structures. However, in order to optimize the operation of the proposed structure, an accurate understanding of the physical behavior and physical phenomena occurring in the device is a must. Two-dimensional (2D) analytical model enables a systematic, fast, physics-based analysis of MOSFET design, a simple 2D analytical model has been developed by solving the 2D Poisson equation and the modeled results are validated using the ATLAS-2D device simulator [18]. The TCAD simulations have been carried out using the ATLAS device simulator running on SUN-BLADE-2000 workstation with two 1.05 GHz UltraSPARC III processors. In the case of simulations, a separate file needs to be run for any change in the structural parameters. The machine takes a computational time of 1928.34 s to evaluate sub-threshold electrical characteristics upto \( I_{ds} - V_{gs} \). However, using the proposed analytical model, the device performance analysis with the same set of structural parameters takes just 60 s to evaluate sub-threshold electrical characteristics.
upto $L_{vgs}$ on a P-IV system having a system frequency of 2.4 GHz. In the TCAD simulation for sub-nanometer devices, the well-known drift-diffusion method is not adequate because it ignores the non-local transport of carriers and the carrier heating. Tools now widely used for simulation of high-bias and small-size devices are the hydrodynamics energy transport model. In our simulation, we adopt the hydrodynamic energy transport model which includes the continuity equations, momentum transport equations, energy balance equations of the carriers and the Poisson equation. It can model the non-local transport phenomenon, and hence presents a higher accuracy than the drift–diffusion method.

We adopt the CONMOB (concentration-dependent mobility) model for low field mobility. In that model, the mobility is only related to the doping density. In high field, we adopt the TMPMOB model, which takes into account the dependence on electric fields both parallel and perpendicular to the direction of current flow, and uses an effective electric field calculated from carrier temperature in the mobility calculations. For the same current flow, and uses an effective electric field calculated from

$$I \text{upto}$$


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2. Model formulation

2.1. Two-dimensional potential and electric field analysis

A schematic structure of MLaG-RC MOSFET is shown in figure 1(a) with a gate length of $L$. The source/drain (S/D) regions are rectangular and uniformly doped at $10^{20}$ cm$^{-3}$. The channel doping concentration (or substrate doping density), $N_{a}$, is also uniform. Assuming the impurity density in the channel region to be uniform, the potential distribution $\psi(x, y)$ in the silicon film in the weak inversion region can be given as

$$\frac{\partial^2 \psi(x, y)}{\partial x^2} + \frac{\partial^2 \psi(x, y)}{\partial y^2} = \frac{q N_{a}}{\varepsilon_{\text{Si}}}$$

for $0 \leq x \leq L_{eff}$ and $(d + \text{EOT}) \leq y \leq (d + \text{EOT} + Y_{d})$

where $\varepsilon_{\text{Si}}$ is the dielectric constant of silicon, $q$ is the electronic charge and $d$ is the groove depth. $Y_{d}$, EOT and $L_{eff}$ are the depletion layer thickness, effective oxide thickness of the gate and the effective channel length respectively; which are defined as follows.

The depletion layer thickness, $Y_{d}$, is approximately given by

$$Y_{d} = \sqrt{\frac{2 \cdot \varepsilon_{\text{Si}}}{q \cdot N_{a}}} \cdot 1.5 \psi_{f},$$

where $\psi_{f}$ is the Fermi potential and is given by

$$\psi_{f} = \frac{K_{B} T}{q} \cdot \ln \left( \frac{N_{a}}{n_{i}} \right),$$

where $n_{i}$ is the intrinsic carrier concentration, $K_{B}$ is the Boltzmann constant and $T$ is the room temperature.

The effective gate oxide thickness, EOT, is given by

$$\text{EOT} = t_{ox1} + \frac{\varepsilon_{ox1}}{\varepsilon_{ox2}} t_{ox2},$$

where $t_{ox1}$ and $t_{ox2}$ are the thicknesses of SiO$_2$ and high-$K$ dielectric layers respectively; and $\varepsilon_{ox1}$ and $\varepsilon_{ox2}$ are the corresponding permittivity of the two gate dielectric layers.

The effective channel length, $L_{eff}$, is given by

$$L_{eff} = L + 2(\text{EOT} + \text{NJD}),$$

where NJD is the negative junction depth defined as $\text{NJD} = d + t_{ox} - X_{i}$ and $X_{i}$ being the junction depths of the S/D regions.

The potential profile in the channel region can be approximated by a simple cubic function as

$$\psi(x, y) = \psi_{S}(x, d + \text{EOT}) + K_{x}(x) \cdot y + K_{y}(x) \cdot y^{3},$$

where $\psi_{S}(x, d + \text{EOT})$ is the surface potential and $K_{x}(x)$, $K_{y}(x)$ and $K_{z}(x)$ are the arbitrary coefficients. In the proposed structure, the flat-band voltage of the gate metal, $M$, is given by

$$V_{fb} = \Phi_{M} - \Phi_{Si},$$

where $\Phi_{M}$ is the metal work function and $\Phi_{Si}$ is the silicon work function given by

$$\Phi_{Si} = \chi_{Si} + \frac{E_{G}}{2q} + \psi_{f},$$

where $\chi_{Si}$ is the electron affinity of silicon and $E_{G}$ is the bandgap of silicon at 300 K. In the analytical model, the corners have been smoothed out in such a way that I, II, III (marked in figure 1(b)) are all equivalent to EOT leading to an underestimation of the position of the corner by $\Delta \xi$. It is found that if $\Delta \xi / L_{eff} < 5\%$, the analytical model results are in close proximity to the simulated results. In our analysis, for NJD = 10 nm and varying the gate lengths from $L = 100$ nm to 40 nm, the error $\Delta \xi / L_{eff}$ varies from 3% to 5%; and for NJD = 30 nm with gate lengths varying from $L = 100$ nm to 40 nm, the error $\Delta \xi / L_{eff}$ varies from 2% to 4%. In the case of gate lengths less than 40 nm, $\Delta \xi / L_{eff}$ becomes greater than 5% and hence the corner effects in modeling cannot be ignored.

The Poisson equation under the gate region is solved using the following boundary conditions:

1. Electric flux at the gate-oxide/Si interface is continuous. Thus

$$\frac{\partial \psi(x, y)}{\partial y} = \frac{V'_{G} - \psi_{S}(x, y)}{\gamma \cdot \text{EOT}}$$

at $0 < x < L_{eff}$ and $y = d + \text{EOT},$

where $V'_{G} = V_{G} - V_{gh}$ where $V_{G}$ is the gate-to-source voltage. $\gamma$ is defined as $\gamma = \frac{\varepsilon_{ox1}}{\varepsilon_{ox2}}$, where $\varepsilon_{ox1}$ is the permittivity of SiO$_2$.

2. Potential at the depletion edge is $V_{sub}$.

$$\psi(x, y) = V_{sub}$$

at $0 < x < L_{eff}$ and $y = d + \text{EOT} + Y_{d},$

where $V_{sub}$ is the substrate bias.

3. Electric field at the depletion edge is zero.

$$\frac{\partial \psi(x, y)}{\partial y} = 0$$

at $0 < x < L_{eff}$ and $y = d + \text{EOT} + Y_{d}$. 
(4) Potential at the source end is
\[ \psi_s(x, y) = V_{ds}, \] \hspace{1cm} \text{at} \hspace{0.5cm} x = 0 \hspace{1cm} \text{and} \hspace{1cm} y = d + \text{EOT}, \] (12)
where \( V_{ds} \) is the built-in voltage.

(5) Potential at the drain end is
\[ \psi_s(x, y) = V_{bn} + V_{ds}, \] \hspace{1cm} \text{at} \hspace{0.5cm} x = L_{eff} \hspace{1cm} \text{and} \hspace{1cm} y = d + \text{EOT}, \] (13)
where \( V_{bn} \) is the applied drain-to-source bias.

Using boundary conditions, i.e., (9)–(13) and substituting into (6), the coefficients \( K_1(x) \), \( K_2(x) \), and \( K_3(x) \) are obtained as
\[ K_1(x) = (V'_s - V_{sub}) \cdot \left[ \frac{-2}{L_1} \frac{4Y_d}{\beta_1} \frac{6}{\beta_2} \right] \]
\[ - (V'_s - \psi_s(x, d + \text{EOT})) \cdot \left[ \frac{2Y_d}{\beta_1} + \frac{(\beta_2^2 - 2\beta_1)C_{ox}}{\varepsilon_s \beta_2} \right], \] (14)
\[ K_2(x) = \frac{(V'_s - V_{sub})}{\beta_1} \cdot \left[ \frac{1}{\beta_1} \frac{4}{\beta_2^2} \right] \]
\[ - (V'_s - \psi_s(x, d + \text{EOT})) \cdot \left[ \frac{2}{\beta_1} \frac{2\beta_1^2 + 4\beta_3}{\beta_2^2 \beta_3} \right]. \] (15)
\[ K_3(x) = (V'_s - V_{sub}) \cdot \left[ \frac{2}{\beta_1} \frac{\beta_1^2 - 2\beta_3}{\beta_2^2 \beta_3} \right] \]
\[ + (V'_s - \psi_s(x, d + \text{EOT})), \] (16)
where \( C_{ox} = \frac{C_{ox}}{EOT} \) is the gate oxide capacitance per unit area and \( \beta_1, \beta_2 \) and \( \beta_3 \) are the constants given by
\[ \beta_1 = d + \text{EOT} + Y_d, \]
\[ \beta_2 = Y_d - 2d - 2\text{EOT}, \]
\[ \beta_3 = \frac{Y_{gs}}{\varepsilon_s Y_d}. \] (17)

Thus, the surface potential \( \psi_s(x, d + \text{EOT}) \) under the gate region can be obtained by substituting (6) into (1) and is given as
\[ \psi_s(x, d + \text{EOT}) = \delta(x) + V'_s - \left[ \frac{qN_a}{\varepsilon_s} - (V'_s - V_{sub}) \right] \]
\[ \times \left[ \frac{2Y_d^2 + 8dY_d + 8 \cdot \text{EOT} \cdot Y_d - 8\beta_1}{\beta_1^2 \beta_2} \right] \] \cdot \xi^2, \] (18)
where \( \xi \) is the device characteristic length defined as
\[ \xi = \sqrt{\frac{\beta_1^2 \beta_2 \beta_3}{-2\beta_2 \beta_3 - 4\beta_1^2 + 6(d + \text{EOT}) \beta_1^2 - 12(d + \text{EOT}) \beta_1}}, \] (19)
and
\[ \delta(x) = \frac{\delta_{D} \cdot \sinh \left( \frac{L_{eff} - x}{\xi} \right) + \delta_{D} \cdot \sinh \left( \frac{x}{\xi} \right)}{\sinh \left( \frac{L_{eff}}{\xi} \right)}. \] (20)

Using the boundary conditions (12) and (13) at source and drain end respectively, \( \delta_s \) and \( \delta_D \) are obtained as
\[ \delta_s = V_{bn} - V'_s \]
\[ + \left[ \frac{qN_a}{\varepsilon_s} + \frac{2Y_d^2 + 8dY_d + 8 \cdot \text{EOT} \cdot Y_d - 8\beta_1}{\beta_1^2 \beta_2} \right] \] \cdot V_{sub} \] \cdot \xi^2 \] \cdot \xi^2, \] (21)
\[ \delta_D = \delta_s + V_{ds}. \] (22)

The surface electric field distribution can be obtained by differentiating the channel potential at the surface (i.e., at \( y = d + \text{EOT} \)) given by (18):
\[ E_s(x) = -\frac{d}{dx} \psi_s(x, d + \text{EOT}) \] (23)
and is found to be expressed as
\[ E_s(x) = \frac{\delta_{D} \cdot \cosh \left( \frac{L_{eff} - x}{\xi} \right) - \delta_{D} \cdot \cosh \left( \frac{x}{\xi} \right)}{\xi \cdot \sinh \left( L_{eff}/\xi \right)}. \] (24)

2.2. Position of minimum surface potential and threshold voltage analysis

The threshold voltage, \( V_{th} \), is defined as the gate-to-source voltage, \( V_{gs} \), at which the minimum surface potential \( \psi_s(x_{\text{min}}, d + \text{EOT}) \) equals \( 2\psi_f \), where \( x_{\text{min}} \) is the position of minimum surface potential and is evaluated by

\[ E_s(x_{\text{min}}) = \left. \frac{d}{dx} \psi_s(x, d + \text{EOT}) \right|_{x = x_{\text{min}}} = 0. \] (25)

The values of \( x_{\text{min}} \) can be evaluated numerically by solving
\[ \cosh \left( \frac{L_{eff} - \xi}{\xi} \right) = \frac{\delta_{D}}{\delta_{s}}. \] (26)

Thus, the corresponding minimum surface potential can be obtained using (18) and (23) as
\[ \psi_s(x_{\text{min}}, d + \text{EOT}) = \delta(x_{\text{min}}) + V'_s - \left[ \frac{qN_a}{\varepsilon_s} - (V'_s - V_{sub}) \right] \]
\[ \times \left[ \frac{2Y_d^2 + 8dY_d + 8 \cdot \text{EOT} \cdot Y_d - 8\beta_1}{\beta_1^2 \beta_2} \right] \] \cdot \xi^2, \] (27)

Hence, substituting \( \psi_s(x_{\text{min}}, d + \text{EOT}) = 2\psi_f \) and \( V_{gs} = V_{th} \) in (27), we obtain the expression for the threshold voltage as
\[ V_{th}(x_{\text{min}}) = \left[ \frac{2}{} \right] + \frac{\left( \frac{qN_a}{\varepsilon_s} + \left( \frac{2Y_d^2 + 8dY_d + 8 \cdot \text{EOT} \cdot Y_d - 8\beta_1}{\beta_1^2 \beta_2} \right) \cdot V_{sub} \right]}{1 + \left( \frac{2Y_d^2 + 8dY_d + 8 \cdot \text{EOT} \cdot Y_d - 8\beta_1}{\beta_1^2 \beta_2} \right) \cdot \xi^2} \]
\[ + V_{th}. \] (28)

Thus, the position of the minimum surface potential is very important in determining the threshold voltage and sub-threshold swing in the device.

2.3. Sub-threshold slope and sub-threshold drain current model

Sub-threshold swing is a pre-requisite in the sub-threshold regime of device operation, to design analog switches [19], low voltage and low standby power dissipation circuits in CMOS technology. Moreover, for a device to have good turn-on or switching characteristics, this device characteristic parameter should be as small as possible. \( S \) can be expressed in terms of minimum surface potential [20] and is given by
\[ S = \frac{2.303 \cdot K_{\mu} T}{q} \frac{1}{\frac{\partial \psi_s(x_{\text{min}}, d + \text{EOT})}{\partial V_{gs}}}. \] (29)
The sub-threshold current is the leakage current that affects the dynamic circuits and determines the standby power consumption in VLSI. The sub-threshold regime mainly describes the switching behavior of the device and is particularly important for low-power applications. It is, thus, essential to maintain good sub-threshold characteristics. The sub-threshold drain current is obtained using the minimum surface potential, which is crucial for low-power applications. It is, thus, important to maintain good sub-threshold characteristics.

\[ I_{th} = \frac{\sqrt{2} \cdot W \cdot \varepsilon_{si} \cdot \mu}{2 \cdot L_{eff}} \cdot \left( \frac{K_BT \cdot n_i}{q \cdot N_a} \right)^2 \]
\[ \times \sqrt{\frac{q^2 N_a \cdot \psi_S(x_{min}, d + EOT)}{(K_BT)^2 \cdot \psi_{Si}} \left[ 1 - \exp \left( \frac{-q \cdot V_{th}}{K_BT} \right) \right] \]
\[ \times \exp \left( \frac{q \cdot \psi_S(x_{min}, d + EOT)}{K_BT} \right) \]

where \( \mu \) is the electron mobility extracted from device simulation [18] using the concentration-dependent low field mobility (CONMOB) model and the parallel electric-field-dependent (FLDMOB) model.

### 3. Results and discussion

In a multi-layered gate dielectric system, an extra-thin low-\( K \) interfacial layer is introduced between the high-\( K \) layer and the silicon layer to improve the interface quality and stability. Thus, due to the continuity of displacement current at the interface of High-\( K \)/SiO\(_2\) system, high fringing fields are focused into the low-\( K \) dielectric layer [5]. This electrical focusing alters the effect of fringing fields on the device performance. The modeled surface potential and electric field distribution with the normalized channel position for MLaG-RC and conventional RC MOSFET designs are shown in figures 2 (a) and (b), along with the simulated results. A close proximity between the modeled and simulated results validates the model. A slight increase in potential barrier near source end is seen for MLaG-RC design (i.e. with higher \( \varepsilon_{ox2} \)). This is due to the increased gate controllability on the inversion charge density achieved using higher \( \varepsilon_{ox2} \). Incorporation of multi-layered high-\( K \) dielectric system facilitates physically thicker gates, thereby permitting the scaling of gate oxide thickness and thus, increasing gate control over the channel. The potential barrier is, however, raised to prevent electron injection from source, in order to maintain a balance between charges in the semiconductor and gate according to MOS electrostatics. Further, figure 2 reflects nearly 13\% lower electric field near the drain end for the proposed design, thus reducing gate leakage current and hence, enhancing the hot carrier immunity. Figure 3 depicts the electron temperature and electron velocity variation, for MLaG-RC and RC MOSFET designs, with the normalized channel position. The hot carriers (i.e. electrons) in the high electric field drain region, as measured in terms of electron temperature, serves as a key for evaluating hot electron-induced device degradation. Results clearly reveal a lower electron temperature near the drain end for the proposed design, about 15.7\% lower than the conventional RC MOSFET, thereby indicating enhancement of hot carrier immunity in the former. Figure 3 also reflects higher carrier transport efficiency near the source end for MLaG-RC MOSFET owing to the use of high-\( K \) upper dielectric, which reduces EOT and hence, enhances gate control over the channel. Figures 4(a) and (b) reflect a good

<table>
<thead>
<tr>
<th>Surface Potential (V)</th>
<th>Electric Field (MV/cm)</th>
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<tbody>
<tr>
<td>MLaG-RC MOSFET</td>
<td>RC MOSFET</td>
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<tr>
<td>( V_{ds} = 0.5V )</td>
<td>( V_{ds} = 0.5V )</td>
</tr>
<tr>
<td>( \varepsilon_{ox} = 20 )</td>
<td>( \varepsilon_{ox} = 3.9 )</td>
</tr>
<tr>
<td>EOT = 1.585nm</td>
<td>EOT = 1.585nm</td>
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Figure 2. Surface potential and electric field variation with the normalized position along the channel (a) for MLaG-RC MOSFET; and (b) RC MOSFET. \( L = 40 \) nm, \( V_{gs} = 0.1 \) V, \( N_a = 5 \times 10^{16} \) cm\(^{-3} \), \( t_{ox} = 4 \) nm.
agreement of modeled and simulated surface potential and electric distribution of MLaG-RC design, along the channel for different drain biases, thereby validating the model results for low- and high-drain biases for sub-50 nm device dimensions.

DIBL and sub-threshold swing are two important parameters to determine the short channel immunity of a device. The relative threshold voltage, subthreshold performance and DIBL of RC structures with and without multi-layered gate dielectric architecture for different NJDs are reflected from figures 5 and 6. It has been observed that as NJD increases, both DIBL and subthreshold slope decrease and the threshold voltage increases. This comes from the fact that as NJD increases, carriers in the channel require higher energy to surmount the potential barrier round the corner, thereby raising the threshold voltage. Higher NJDs, however, provides better switching due to reduced sub-threshold swing. A trade-off can, thus, be made depending upon the design requirements whether the threshold voltage is the need of the design or is it the switching behavior. Further, it is evident from the inset of figure 6 that the threshold voltage decreases with increasing upper gate oxide dielectric (i.e. $\varepsilon_{ox2}$). This is mainly attributed to an increase in surface potential, as a result of the charges induced in the drain and source regions because of fringing field lines from the bottom of the gate electrode. This leads to an early onset of inversion in the channel; thereby lowering the threshold voltage. The drop in the threshold voltage is as high as about 15–20 mV for $L = 40$ nm when $\varepsilon_{ox2}$ increases from 3.9 to 50. The recessed gate nature of the device, further, minimizes the DIBL and punchthrough effects due to reduction
in the lateral field penetration from the source/drain region. This lateral penetration of the field is further enhanced with the use of gate stack, as is evident from the results shown in figures 5 and 6. This is due to the improved gate control over the channel with the multi-layered gate dielectric system (High-κ/SiO₂) thus, proving the design efficacy for logic and switching applications. The consistency between our model results and those in the ATLAS-2D device simulation verifies the accuracy of the analytical model.

The sub-threshold drain current characteristics of both MLaG-RC and conventional RC MOSFETs are shown in figures 7(a) and (b) respectively, along with their ON current to OFF current ratio (ION/IOFF). The ION/IOFF values mentioned in figure 7–10 have been obtained through device simulation. Figures 7(a) and (b) demonstrate that although MLaG-RC structure exhibits nearly the same drain current in the sub-threshold regime, i.e. the off-state leakage current, as compared to conventional RC MOSFET, the proposed design shows a significant on-state current enhancement in terms of higher ION/IOFF. This performance enhancement is mainly because of the increased gate controllability over the channel due to the multi-layered high-κ gate architecture that reduces the EOT. An improved switching characteristic, with the proposed design, has also been observed clearly from ION/IOFF values specified in figures 7(a) and (b). The effect of drain bias on the drive current performance of the proposed design has also been illustrated in figure 7(c), indicative of the fact that a higher drive current can be achieved by increasing the drain bias. The effect of the upper gate oxide dielectric (i.e. εox2) on the drive current performance has been studied in figure 8. Results reveal that increasing εox2 enhances the on-state drive current without degrading the off-state leakage current; and hence improving the device switching behavior as is clear from ION/IOFF values specified in figure 8.
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1.0E-13
1.0E-11
1.0E-09
1.0E-07
1.0E-05
1.0E-03
0 0.3 0.6 0.9 1.2 1.5
Gate-to-Source Voltage, Vgs (V)

Drain Current, log (Ids) (A/µm)

MLaG-RC MOSFET
Lg = 40nm
Vds = 0.1V
NJD = 20nm

Figure 8. Drain current characteristics of MLaG-RC MOSFET, with the applied gate-to-source voltage for two different upper gate oxide dielectrics in the logarithmic scale; calculated from the analytical model and compared with ATLAS-2D simulated results in the sub-threshold regime. Simulated values of ION/IOFF have also been mentioned. Ns = 1 x 10^{17} cm^{-3} and taox = 4 nm.

1.0E-14
1.0E-12
1.0E-10
1.0E-08
1.0E-06
1.0E-04
1.0E-02
0 0.3 0.6 0.9 1.2 1.5
Gate-to-Source Voltage, Vgs (V)

Drain Current, log (Ids) (A/µm)

MLaG-RC MOSFET
Lg = 40nm
Vds = 0.1V
NJD = 10nm
NJD = 30nm

Figure 9. Drain current characteristics of MLaG-RC MOSFET, with the applied gate-to-source voltage for two different negative junction depths in the logarithmic scale; calculated from the analytical model and compared with ATLAS-2D simulated results in the sub-threshold regime. Simulated values of ION/IOFF have also been mentioned. Ns = 1 x 10^{17} cm^{-3} and taox = 4 nm.

doping on the drive current performance of MLaG-RC design has also been studied as shown in figure 10. Increase in the channel doping, increases the device’s threshold voltage leading to drive current degradation and hence, deteriorating the switching characteristics in terms of ION/IOFF.

The present work also provides valuable design insights in the performance of nanoscale MLaG-RC MOSFET and hence serves as a tool to optimize important device and technological parameters in the sub-50 nm regime of operation. Figure 11 shows that the sub-threshold performance is improved by increasing the groove depth. For a device with a higher groove depth, lower substrate doping is required to achieve improved sub-threshold performance as is clear from figure 12. Results also reflect that in order to achieve better device switching from OFF state to ON state, the analyzed device should be designed with a high threshold voltage, thereby providing optimization for high-performance switching applications. Further, figure 12 predicts that a higher substrate doping is required to achieve higher Vth and hence, the improved sub-threshold performance. Figure 13 shows NJD variation with S/D junction depths for different groove depths. Results indicate that a lower S/D junction depth proves to be beneficial in terms of higher NJD; thus, boosting the corner effects and hence, resulting in the punchthrough and DIBL reduction as is clear from figure 6. Higher NJD, on the other hand, also increases the device’s threshold voltage and degrades the driving current due to potential barriers augmentation at the corners with increase in NJD. Thus,
careful engineering of S/D junction depths, NJDs and groove depths can achieve an optimal high-performance device design in terms of short channel effect immunity and hot carrier effect immunity. Properly optimized lower NJD (or lower groove depth) combined with low-substrate doping design can improve the device analog performance, unlike the case for logic and switching applications where a higher NJD is desired. Figure 13 (inset) predicts NJD variation with the upper gate oxide permittivity for MLaG-RC MOSFET design for four different groove depths (analytical). L = 40 nm, $N_d = 1 \times 10^{17} \text{cm}^{-3}$ and $t_{ox} = 4 \text{nm}$.

4. Conclusion

We have developed and analyzed a 2D analytical sub-threshold model for the proposed MLaG-RC MOSFET design; and hence, presenting it as an attractive solution for the ongoing integration process in analog and digital design technology. Continued scaling of SiO$_2$-based gate dielectrics necessitates the introduction of high-$K$ materials for sub-50 nm technology node. Results reveal that MLaG-RC design is superior to RC design in all aspects providing superior performance in terms of reduced DIBL, $S$ and $V_{th}$; and improved on-state drive current without degrading the off-state leakage current. Device performance of MLaG-RC MOSFET design can be enhanced further by tuning the device parameters such as $\varepsilon_{ox_2}$, $N_d$ and NJD. The proposed MLaG-RC design, hence, presents its applicability for high speed logic and low standby power (LSP) applications.

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