TCAD Assessment of Gate Electrode Workfunction Engineered Recessed Channel (GEWE-RC) MOSFET and Its Multilayered Gate Architecture—Part I: Hot-Carrier-Reliability Evaluation

Rishu Chaujar, Student Member, IEEE, Ravneet Kaur, Manoj Saxena, Senior Member, IEEE, Mridula Gupta, Member, IEEE, and R. S. Gupta, Senior Member, IEEE

Abstract—This paper discusses a hot-carrier-reliability assessment, using ATLAS device simulation software, of a gate electrode workfunction engineered recessed channel (GEWE-RC) MOSFET involving an RC and GEWE design integrated onto a conventional MOSFET. Furthermore, the impact of gate stack architecture and structural design parameters, such as gate length, negative junction depth, substrate doping ($N_A$), gate metal workfunction, substrate bias, drain bias, and gate oxide permittivity on the device behavior of GEWE-RC MOSFET, is studied in terms of its hot-carrier behavior in Part I. Part II focuses on the analog performance and large signal performance metrics evaluation in terms of linearity metrics, intermodulation distortion, device efficiency and speed-to-power dissipation design parameters, and the impact of gate stack architecture and structural design parameters on the device reliability. TCAD simulations in Part I reveal the reduction in hot-carrier-reliability metrics such as conduction band offset, electron velocity, electron temperature, hot-electron-injected gate current, and impact-ionization substrate current. This paper thus optimizes and predicts the feasibility of a novel design, i.e., GEWE-RC MOSFET for high-performance applications where device and hot-carrier reliability is a major concern.

Index Terms—ATLAS-2D, gate electrode workfunction engineered (GEWE), hot-carrier reliability, negative junction depth (NJD), recessed channel (RC) MOSFET.

I. INTRODUCTION

THE SEARCH for higher performance of ICs has led to the scaling of MOSFETs down to sub-50 nm and below. The hot-carrier deterioration becomes a stringent limitation to the reliability of sub-50-nm devices and VLSI packing density. Technologists use the hot-carrier-reliability and linearity-distortion issues from the device design perspectives. Hot-carrier reliability of MOS devices has been studied as a major reliability concern [1]–[5] for the past several decades since the deeply scaled MOS device design suffers from a hot-carrier effect and also degrades analog circuit requirements. As devices are scaled, the benefits of higher electric fields saturate while the associated reliability problems get worse [6]. The presence of large electric fields in MOSFETs implies the presence of high energy carriers or the hot carriers, in such devices, that might get injected into the surrounding dielectric films such as the gate and sidewall oxides [7]. The presence of mobile carriers in the oxides triggers various undesirable physical processes that drastically change the device characteristics during normal operation over prolonged periods of time eventually causing the circuit malfunctioning. The deteriorating effect of gate leakage current and substrate current on the digital and analog device performance has also been discussed recently [8], [9]. It is thus increasingly important to analyze hot-carrier reliability in terms of hot-electron-injected gate current, impact-ionization substrate current, and electron velocity and temperature near the drain end for their impact on the overall chip performance, and not just for their impact on device speed, because chip-level power constraints as well as device and process variability and reliability can seriously diminish the value of device innovations. Furthermore, linearity has been an important figure of merit (FOM) in all RF and wireless applications to guarantee minimum signal distortion in modern communication systems [10]–[14]. With the drastic increase in the demands for mobile communication and wireless systems, linear and low-noise system designs have become potential solutions to achieve high-quality system performance for system-on-chip (SoC) designs. Linearity and intermodulation distortion analysis and simulation are thus needed to realize the linearity limiting factors for a given technology as well as to optimize transistor structure and device topology for improved performance. The metrics used in this paper to evaluate the device linearity performance and intermodulation distortion are $V_{IP2}$, $V_{IP3}$, and third-order intermodulation distortion $[15]–[17]$. 

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II. RC DEVICE DESIGNS: GATE ELECTRODE WORKFUNCTION AND GATE DIELECTRIC ENGINEERING

As the MOSFET dimensions scale down to sub-50-nm regime, further scaling down of SiO$_2$ gate dielectric leads to high direct tunnelling gate leakage current, which, in turn, causes the increase in device power consumption. This critical issue necessitates the introduction of high-$k$ materials for sub-50-nm technology node so that the physical thickness of oxide layer ($t_{ox} = t_{ox1} + t_{ox2}$) increases, keeping the effective oxide thickness (EOT) same [18]–[21]. The CMOS transistors designed with multilayer high-$k$ gate dielectrics achieve the expected high drive current performance and lower leakage current, thereby proving its efficacy for high-performance CMOS logic applications. The metal gate/high-$k$ dielectric and SiO$_2$ multilayered gate architecture exhibit negligible gate oxide leakage and channel mobilities close to SiO$_2$ [18], [21].

Fig. 1. Schematic cross-sectional view of (a) RC, (b) GEWE-RC, (c) MLaG-RC, and (d) MLGEWE-RC MOSFET designs.

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TABLE I
DEFAULT DESIGN PARAMETERS USED IN THE ANALYSIS FOR VARIOUS RC DEVICE DESIGNS

<table>
<thead>
<tr>
<th>Design Parameters for RC Device Designs</th>
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<tbody>
<tr>
<td>Channel Length ($L_{ch} = L_{G1} + L_{G2}$)</td>
<td>50 nm ($L_{G1} = L_{G2} = 25$ nm)</td>
</tr>
<tr>
<td>Device Width (W)</td>
<td>1 μm</td>
</tr>
<tr>
<td>Groove Depth, (d)</td>
<td>80 nm</td>
</tr>
<tr>
<td>Source/Drain Junction Depth ($X_s$)</td>
<td>74 nm</td>
</tr>
<tr>
<td>Negative Junction Depth (NJD)</td>
<td>10 nm</td>
</tr>
<tr>
<td>Substrate Doping ($N_A$)</td>
<td>1.0 $10^{17}$ cm$^{-3}$</td>
</tr>
<tr>
<td>Source/Drain Doping ($N_D$)</td>
<td>1.0 $10^{20}$ cm$^{-3}$</td>
</tr>
<tr>
<td>Physical Oxide Thickness ($t_{ox}$)</td>
<td>4 nm ($t_{ox1} = t_{ox2} = 2$ nm)</td>
</tr>
<tr>
<td>Permittivity of SiO$_2$</td>
<td>$e_{ox}$</td>
</tr>
<tr>
<td>Permittivity of High-K</td>
<td>$e_{ox2}$</td>
</tr>
<tr>
<td>Effective Oxide Thickness (EOT)</td>
<td>$EOT = e_{t_0} + \frac{e_{ox1} E_{ox1}}{e_{ox2} E_{ox2}}$</td>
</tr>
<tr>
<td>Substrate Bias ($V_{SUB}$)</td>
<td>0 V</td>
</tr>
<tr>
<td>Drain Bias ($V_{DS}$)</td>
<td>1 V</td>
</tr>
<tr>
<td>For RC &amp; MLGaRC MOSFETs</td>
<td>Work function ($\phi_{m1}$) = 4.77 V</td>
</tr>
<tr>
<td>For GEWE-RC &amp; MLGEWE-RC MOSFETS</td>
<td>Workfunction ($\phi_{m1}$) = 4.77 V &amp; ($\phi_{o1}$) = 4.10 V</td>
</tr>
</tbody>
</table>

The design parameters, as discussed above, are the default parameters used in the analysis, unless otherwise stated.

analog and large signal performance; and the impact of gate stack architecture and other structural design parameters such as gate length, NJD, $N_A$, $V_{SUB}$, $V_{DS}$, $e_{ox2}$, and metal gate workfunction variation on the device evaluation metrics.

In the simulation for sub-50-nm gate length devices, the drift-diffusion model is not acceptable since it ignores the nonlocal transport of carriers and the carrier heating. In our simulation, we have adopted the hydrodynamic energy transport model which includes the continuity equations, momentum transport equations, energy balance equations of the carriers, and the Poisson equation. It can model the nonlocal transport phenomenon and is more accurate than the drift-diffusion method. In the study of gate and substrate currents, the impact-ionization and hot-electron-injection models are used to provide an accurate measure of hot-carrier-injection fluxes in short-channel MOS technologies. All the simulations have been performed using physical models accounting for the electric-field-dependent and concentration-dependent carrier mobilities, Shockley–Read–Hall recombination/generation with doping-dependent carrier lifetime, and Auger recombination. The mobility model used is the inversion layer Lombardi CVT mobility model, wherein concentration-dependent mobility, high field saturation model, and mobility degradation at interfaces are all included [36]. Default simulator coefficients for all parameters have been employed. In order to fairly analyze the device performances, all the four devices are optimized to have the same parameter variations on the device performance. This is because by changing the gate length and NJD, the effective channel length [34] would change, and as a result, the position along the channel will also vary in comparison to other structural parameter variations. Thus, in order to study the impact of all the structural parameter variations w.r.t. one another on a single platform, the position along the channel has been normalized. Furthermore, in all the curves where normalization has been carried out, $x = 0$ represents the source end and $x = 1$ represents the drain end.

III. DEVICE FABRICATION FEASIBILITY

As predicted by the device designers, device performance deterioration becomes a stringent limitation as the devices are scaled down to sub-50-nm regime. Hence, in order to improve and enhance the life span of conventionally scaled MOSFET designs, various designs are approaching the device realization scenario. The work thus supplements this precondition by proposing and investigating the hot-carrier reliability, linearity-intermodulation issues, and analog device performance of GEWE-RC MOSFET employing various engineering schemes, namely, lateral channel engineering by using RC and gate electrode workfunction engineering by using DMG architecture. In addition to this, study has also been carried out to investigate the impact of gate stack architecture on the device performance of GEWE-RC MOSFET. From the simulation study using ATLAS device simulator [36], it has been shown that the upshot of these engineering combinations can boost the hot-carrier reliability (discussed in Part I), and the linearity-intermodulation issues and analog device performance (discussed in Part II) of conventional devices.

For the feasibility of RC MOSFET structure, several integration schemes have been suggested such as plasma etching and LOCOS isolation [23], reactive ion etching and LOCOS isolation technique [24], self-aligned chemical–mechanical polishing (CMP) where the self-aligned process was defined by the groove etching and polysilicon CMP steps [37], and shallow trench isolation where gate oxide films were produced with a conventional furnace and the oxide films for gate electrode were deposited by LP-CVD at 850 °C [38]. For the feasibility of DMG architecture, the various available integration schemes are tilt angle evaporation metal gate deposition [22], metal interdiffusion process [39], [40], CMP [41], and fully silicided metal gate [42]. To add further, in 2006, Na and Kim [43] have successfully fabricated DMG architecture by poly-Si gate doping control of the source and drain side gate individually. Moreover, in addition to this, fabrication schemes are also available for high-$k$ gate stack architectures such as reactive sputtering and oxidation [40], atomic layer deposition technique [44], and plasma nitridation coupled with metal-organic chemical vapor deposition [45]. The MLGEWE-RC MOSFET [Fig. 1(d)] is thus proposed with optimistic outlook. The technical manufacturing feasibility of MLGEWE-RC MOSFET is not far reaching in the light of various integration schemes discussed earlier. As mentioned by Xiao-Hua et al. [37], by adopting the reactive ion etching and electron beam lithography techniques, the RC architecture implementation into the MOS devices...
still provides excellent short-channel and hot-carrier-effect immunities. The fabrication process flow for the RC structure is compatible with most of the existing CMOS processes. Thus, the performance enhancements such as SCE suppression and hot-carrier-effect immunity obtained from the RC structure can be easily achieved using a process flow that is not much more complicated than that used for fabricating the conventional planar devices. Moreover, a double-recessed heterostructure is compatible with most of the existing CMOS processes. Thus, the proposed device designs also possess superior hot-carrier-reliability. Furthermore, we also investigate the impact of structural design parameters such as gate length, NJD, $N_A$, $V_{SUB}$, $V_{DS}$, $\varepsilon_{ox2}$, and metal gate workfunction ($\Phi_M$) on the hot-carrier efficiency of various device designs.

### IV. RESULTS AND DISCUSSION

Recently [47], [48], we reported that the proposed designs exhibit significant performance enhancement in comparison to the conventional RC MOSFET in terms of improved drain current, drain-induced barrier lowering (DIBL), threshold voltage, intrinsic gain, device efficiency, and early voltage for low-power low-voltage analog circuit applications, and switching characteristics in terms of $I_{ON}/I_{OFF}$, subthreshold slope, and high-speed digital and switching applications. The dependence of various performance parameters had also been demonstrated earlier [47] for different values of $L_G1/L_G2$. In this paper, we compare RC, MLaG-RC, GEWE-RC, and MLGEWE-RC MOSFETs with the bulk MOSFET and demonstrate that the proposed device designs also possess superior hot-carrier-reliability.

#### A. Hot-Carrier-Reliability Evaluation

1) **Conduction Band Energy and DIBL:** The hot-carrier reliability is becoming a limiting factor in realizing the sub-50-nm level technology. For the prediction of device performance and for the optimization of MOS devices, the hot-carrier-degradation effects are of paramount importance. The reliability degradation is due to the high electric field near the drain end as the device dimensions are reduced and leads to the degradation of MOSFET current drive capability. However, aggressive scaling of the gate lengths has rendered hot-carrier-injection-induced performance degradation of MOSFETs. Furthermore, as MOSFET dimensions shrink to the sub-50-nm regime, DIBL becomes more prominent. The DIBL effect is found to be more pronounced in bulk devices (barrier lowering, $\Delta\Psi_{BULK} = 44$ mV, which is evaluated as the difference of conduction band energy between $V_{DS}$ of 1.0 and 0.5 V) in comparison to RC and GEWE-RC, as shown in Fig. 2(a), having $\Delta\Psi_{RC} = 40$ mV and $\Delta\Psi_{GEWE} = 25$ mV, respectively, resulting in a higher electrostatic coupling. Significant barrier lowering in bulk leads to leakage current (due to drain bias) [4] just below the gate and, hence, can result in increased power dissipation. However, GEWE-RC MOSFET exhibits step conduction band energy profile in the channel due to metal gate workfunction difference. This screens the region near the source from the drain bias variations and hence accounts for lowest DIBL, showing better control of SCEs over conventional RC and bulk devices. This screening effect is improved significantly at higher $V_{GS}$, in comparison to bulk. This is due to the improved gate control of the device over the channel, thereby decreasing the impact of drain bias on the potential barrier. As shown in Fig. 2(b), bulk MOSFET exhibits $\Delta\Psi_{BULK} = 204$ mV, whereas for GEWE-RC MOSFET, $\Delta\Psi_{GEWE} = 58$ mV, thereby reflecting significant SCE immunity. Fig. 2(c) shows the impact of tuning the GEWE architecture in terms of NJD, $\Phi_M$, $V_{SUB}$, and $N_A$ on the barrier height. An increase of potential barrier near the source end is seen for higher NJD. This is due to the fact that potential barrier at the corners increases with the increase in NJD, and hence, the carriers now require higher energy to surmount the barriers, thereby deteriorating the current driving capability. No effective barrier lowering is seen for $\Phi_M$ variations, but upon increasing screening gate metal workfunction ($\Phi_M$), smaller step in conduction band energy profile at the interface between two metals is seen, which affects the drain bias screening of $M1$. Furthermore, with an increase in the substrate doping and substrate bias, the resulting body effect degrades the driving efficiency.

### TABLE II

<table>
<thead>
<tr>
<th>Summary of the Standard CMOS Process Flow With MLGEWE-RC Implementation</th>
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<tr>
<td><strong>Starting Material:</strong> p-type substrate</td>
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<tr>
<td><strong>Well Diffusion &amp; Active Region Definition</strong></td>
</tr>
<tr>
<td><strong>Drive-In Diffusion &amp; Gate Oxidation</strong></td>
</tr>
<tr>
<td><strong>Source/Drain Implantation and Anneal</strong></td>
</tr>
<tr>
<td><strong>Groove Etching by a combination of Electron Beam Lithography &amp; Reactive Ion Etching</strong> [37]</td>
</tr>
<tr>
<td><strong>SiO$_2$ Implantation at the bottom of the Groove and Annealing</strong> [37]</td>
</tr>
<tr>
<td><strong>High-K Layers Deposition Using Atomic Layer Deposition Technique &amp; Post Deposition Annealing</strong> [45]</td>
</tr>
<tr>
<td><strong>Precise Tilt Angle Evaporation Technique: Metal Gate 1 Deposition &amp; Normal Evaporation: Metal Gate 2 Deposition</strong> [27]</td>
</tr>
<tr>
<td><strong>Contact Etch and Metal Deposition</strong></td>
</tr>
<tr>
<td><strong>Continue Processing</strong></td>
</tr>
</tbody>
</table>
Fig. 2. (a) Conduction band energy variation along the channel at a depth of 1 nm below Si/SiO$_2$ interface for $V_{GS} = 0$ V for GEWE-RC, RC, and bulk devices at $V_{DS} = 0.5$ and 1.0 V. $x = 0$ represents the source end, and $x = 1$ represents the drain end. Design parameters for bulk MOSFET in all the figures are $L_G = 50$ nm, device width ($W$) = 1 $\mu$m, $X_j = 74$ nm, $N_A = 1 \times 10^{17}$ cm$^{-3}$, source/drain doping, $N_{+D} = 1 \times 10^{20}$ cm$^{-3}$, $t_{ox} = 4$ nm, and $\varepsilon_{ox} = 3.9$. (b) Conduction band energy variation along the channel at a depth of 1 nm below Si/SiO$_2$ interface for $V_{GS} = 0.5$ V for GEWE-RC, RC, and bulk devices at $V_{DS} = 0.5$ and 1.0 V. (c) Conduction band energy variation with the normalized position along the channel for GEWE-RC MOSFET for different NJD, screening metal gate workfunction ($\phi_{M2}$), substrate bias ($N_A$), and substrate bias ($V_{SUB}$) for $V_{GS} = 0.0$ V. (d) Conduction band energy variation along the channel at a depth of 1 nm below Si/SiO$_2$ interface for $V_{GS} = 0$ V for MLGEWE-RC and MLaG-RC devices at $V_{DS} = 0.5$ and 1.0 V. (Inset) Conduction band energy variation with the normalized position along the channel for MLGEWE-RC MOSFET for different $\varepsilon_{ox2}$.

capability due to the raised potential barriers. Fig. 2(d) reflects the impact of multilayered gate stack architecture on the device performance of RC and GEWE-RC MOSFETs, resulting in new structures termed as MLaG [Fig. 1(c)] and MLGEWE-RC MOSFETs [Fig. 1(d)]. As is clear from the results, the screening of the channel region from drain bias variations is tremendously increased with the gate stack architecture. With MLaG-RC and MLGEWE-RC, due to improved gate controllability over the channel, DIBL is significantly lowered, resulting in $\Delta \Psi_{MLaG} = 32$ mV and $\Delta \Psi_{MLGEWE} = 19$ mV. The inset in Fig. 2(d) reflects that on increasing the upper gate oxide permittivity $\varepsilon_{ox2}$ from 10 to 20, which further reduces DIBL, resulting in $\Delta \Psi_{MLGEWE} = 13$ mV. This is mainly due to the decrease in EOT that results in an improved gate control on the inversion charge density. This is further reflected in Fig. 3 where the DIBL effect is reduced with gate stack architectures. Moreover, with the increase in the applied drain to source bias, the DIBL effect increases, but this increase is significant in bulk and RC MOSFETs in comparison to the proposed designs, mainly due to improved gate control in the latter.

2) Electron Velocity and Electron Temperature Distribution: Fig. 4(a)–(e) predicts the electron velocity variation of bulk, RC, GEWE-RC, MLaG-RC, and MLGEWE-RC MOSFET designs, with the normalized position along the channel. In order to improve the carrier injection, i.e., carrier transport efficiency...
in the channel, the electron velocity near the source should be more than near the drain. Significantly higher electron velocity (3.2 \times 10^7 \text{ cm/s}) near the source side is obtained for GEWE-RC in contrast to 0.8 \times 10^7 and 0.03 \times 10^7 \text{ cm/s} obtained for RC and bulk, respectively, as shown in Fig. 4(a)–(c), thereby enhancing the source carrier injection appreciably into the channel. In the GEWE architecture, due to the amalgamation of two gate metals of different workfunction, a peak in the
electric field occurs at the $M_1 - M_2$ interface [47] that causes a more uniform electric field distribution along the channel, resulting in a larger average velocity when the electrons enter into the channel from the source. Thus, the peak electric field underneath the gate has the advantage of improved gate control over the channel, thereby enhancing the carrier transport efficiency and, hence, the electron velocity near the source end [49], [50]. Moreover, incorporating the multilayered gate architecture onto the RC and GEWE-RC MOSFETs results in a significant improvement in the electron velocity near the source (9.0 × 10^7 cm/s for MLaG-RC and 10.8 × 10^7 cm/s for MLGEWE-RC), due to improved gate controllability over the channel owing to higher electric field peak underneath the gate [51], hence leading to higher carrier transport efficiency and current driving capability. Furthermore, Fig. 4 also shows that a lower electron velocity of 0.04 × 10^7 cm/s near the drain end is obtained for MLGEWE-RC MOSFET in contrast to 0.6 × 10^7 cm/s, 1.3 × 10^7 cm/s, 2.1 × 10^7 cm/s, and 2.5 × 10^7 cm/s observed for MLaG-RC, GEWE-RC, RC, and bulk, respectively, providing excellent hot-carrier immunity.

Fig. 5(a)–(e) predicts the electron temperature variation of bulk, RC, GEWE-RC, MLaG-RC, and MLGEWE-RC MOSFETs, respectively, with the normalized position along the channel. The electron temperature gradient, i.e., $\delta T/\delta (x/L)$, as the carriers move from source to drain, is reduced significantly with GEWE-RC MOSFET design in comparison to the conventional RC and bulk MOSFETs. $\delta T/\delta (x/L)$, as evaluated 10% away from the drain (toward the source), gives a remarkable reduction in electron temperature to 1290 K in GEWE-RC MOSFET from 6480 K in RC and 7660 K in bulk MOSFETs as shown in Fig. 5(a)–(c). Due to the corners present in the RC structure, the electron temperature also falls down abruptly at the corners, thereby significantly enhancing the hot-carrier immunity of the device. Fig. 5(d) and (e) predicts the impact of multilayered gate architecture on the electron temperature of RC and GEWE-RC MOSFETs. As is clear from the results, an appreciable reduction in the electron temperature gradient for MLaG-RC ($\delta T/\delta (x/L) = 4570$ K) and MLGEWE-RC ($\delta T/\delta (x/L) = 160$ K) is obtained due to improvement in the gate control over the channel, thus proving excellent hot-carrier reliability of the device.

3) Impact-Ionization Substrate Current and Hot-Carrier-Injected Gate Current: For SoC and high-speed logic applications, device degradation is mainly attributed to the existence of impact-ionization substrate current ($I_{\text{II-I}_{\text{SUB}}}$) and hot-electron-injected gate current ($I_{\text{HE-I}_{\text{G}}}$). Reduced substrate and gate currents can significantly improve the device speed performance and, hence, can reduce the power dissipation. The hot-carrier-injection gate current and the impact-ionization substrate current accurately reflect the hot-carrier-effect reliability and, hence, are used as the hot-carrier-reliability indices. During the study on the gate current, we have adopted the hot-electron-injection model, and for the substrate-current simulations, impact-ionization model was considered. Fig. 6(a) shows that $I_{\text{HE-I}_{\text{G}}}$ in GEWE-RC MOSFET is reduced significantly in comparison to its conventional bulk and RC MOSFET counterparts, as the devices are scaled down to sub-50 nm or even lower. The main factor resulting in smaller hot-carrier effects in RC devices is the corner effects. When the carriers move across the channel from source to drain, they have to surmount the potential barriers formed at the two corners. The hot-carrier-injection gate current in RC devices is appreciably reduced consequentially. Moreover, on reducing NJD (by reducing groove depth, keeping the S/D junction depth constant), the screening
Fig. 6. (a) Hot-carrier-injection gate current in GEWE-RC, RC, and bulk MOSFETs explaining gate length and NJD variation for \( V_{DS} = 1.0 \) V. (b) Hot-carrier-injection gate current in GEWE-RC MOSFET describing the effect of various technological parameters such as metal workfunction \( \Phi_{M2} \) and substrate doping \( N_A \) for different substrate bias \( (V_{SUB}) \) and drain bias \( (V_{DS}) \) voltages. (c) Impact of multilayered gate architecture on hot-carrier-injection gate current in RC and GEWE-RC MOSFETs. (d) Hot-carrier-injection gate current in MLGEWE-RC MOSFET describing the effect of different \( \varepsilon_{ox2} \).

provided to the carriers by the potential barriers at the corners reduces, which hence deteriorates the hot-carrier reliability. Fig. 6(b) shows the impact of tuning the GEWE architecture in terms of \( \Phi_{M2}, V_{DS}, V_{SUB}, \) and \( N_A \) on HE-I\(_G\). As \( \Phi_{M2} \) increases (or the workfunction difference decreases), the hot-carrier-injected gate current increases due to the reduction in the screening of channel region from drain bias variations and, hence, aggravating DIBL and hot-carrier effects. Moreover, with the increase in the substrate bias and substrate doping, the existent body effect in the device rises, hence depreciating HE-I\(_G\). Furthermore, higher drain bias also degrades the gate leakage current due to higher electric fields near the drain end.

Fig. 6(c) explains the impact of the multilayered gate architecture on HE-I\(_G\). MLaG-RC and MLGEWE-RC MOSFET designs exhibit significantly reduced HE-I\(_G\) due to higher gate control over the channel, resulting in improved current driving capability and lower leakages. Further increasing \( \varepsilon_{ox2} \) increases gate controllability over the channel, resulting in a significant HE-I\(_G\) reduction as shown in Fig. 6(d). MLGEWE-RC MOSFET, thus, is a promising candidate to counteract large gate leakages and increased standby power consumption.

II-I\(_{SUB}\) is one of the important components of the off-state leakage current as mentioned by Semenov et al. [52]. The generation of hole current due to impact ionization leads to a significant increase in substrate current. Substrate current thus provides a good monitor to the heating of the channel carriers and to the electric field in the drain region. Fig. 7(a) shows that the impact-ionization substrate current in GEWE-RC MOSFET is reduced significantly in comparison to its conventional bulk and RC MOSFET counterparts. Furthermore, when the MOS devices are scaled down to sub-50 nm or even lower, the substrate current increases due to deteriorated hot-carrier effects. Moreover, on reducing NJD, the screening provided to the carriers by the potential barriers at the corners reduces, which further deteriorates the substrate current and, hence, the hot-carrier reliability. Fig. 7(b) shows the effect of tuning the GEWE architecture in terms of \( \Phi_{M2}, V_{DS}, V_{SUB}, \) and \( N_A \) on II-I\(_{SUB}\). The results depict that upon increasing \( \Phi_{M2}, \) II-I\(_{SUB}\) increases due to the reduction in the screening of channel region from drain bias variations and, hence, deteriorating DIBL and hot-carrier effects. Moreover, as the substrate bias and substrate doping increase, the body effect in the device rises, resulting in a higher II-I\(_{SUB}\). Also, the substrate current increases with increasing drain bias, indicating strong hot-carrier generation by impact ionization. Fig. 7(c) explains the impact-ionization substrate current in MLaG-RC and MLGEWE-RC MOSFETs. MLaG-RC and MLGEWE-RC MOSFET designs exhibit appreciably reduced II-I\(_{SUB}\) due to higher gate control over the channel, resulting in improved current driving capability and lower leakages. Further increasing \( \varepsilon_{ox2} \) increases gate control over the inversion charge layer, resulting in a significant II-I\(_{SUB}\) reduction as shown in Fig. 7(d). This impact-ionization...
behavior is further reflected by the current density contours for all the devices near the drain end, as shown in Fig. 8(a)–(e). When a high $V_{DS}$ and no gate bias are applied, i.e., the device is in the OFF-state, the current density near the drain end is reduced appreciably in the proposed MLGEWE-RC MOSFET design in comparison to the bulk MOSFET where the impact-ionization effect is significantly higher. Higher electron current density near the drain end at a high $V_{DS}$ reflects appreciable impact ionization. Moreover, as shown in Fig. 9, the impact-ionization substrate current becomes more important as the drain bias is increased due to the increase of the electric field and current density near the drain region. The results thus demonstrate that MLGEWE-RC MOSFET exhibits the lowest impact-ionization substrate current in contrast to the
conventional bulk MOSFET proves its superior hot-carrier efficiency. For low-power and low-voltage analog circuit applications, low II-I, HE-I, and lower electron velocity and temperature near the drain end are important design parameters. With proper choice of various structural parameters like $\varepsilon_{ox2}$, $\Phi_{M2}$, and NJD, II-I, and HE-I can be appreciably lowered, as shown in Figs. 6 and 7.

V. CONCLUSION

The framework presented here represents an essential component of technological design process for building hot-carrier reliable device design, in current and future technologies. In this paper, we emphasize our focus on gate electrode work-function engineering and RC architecture incorporation onto the conventional bulk MOSFET for improved hot-carrier reliability of scaled MOS devices. Moreover, the impact of gate stack architecture has also been studied on the performance of GEWE-RC MOSFET design. Intensive 2-D device simulations have been performed to explore the internal transport conditions of RC, GEWE-RC, MLaG-RC, and MLGEWE-RC MOSFETs, and substantial interpretation is given to the internal behaviors observed in all the devices investigated. A comparison of the FOMs for hot-carrier efficiency of bulk, RC, GEWE-RC, MLaG-RC, and MLGEWE-RC MOSFETs was also carried out. Furthermore, the reduction in hot-electron-injected gate current, electron velocity and electron temperature near the drain end, and impact-ionization substrate current is achieved with GEWE-RC MOSFET, thereby enhancing the hot-carrier reliability of the device. Using higher metal workfunction difference and $\varepsilon_{ox2}$, along with lower NJD, tremendously enhances the short-channel immunity offered by GEWE-RC MOSFET, owing to greater gate controllability over the channel. GEWE-RC MOSFET hot-carrier immunity can further be improved by careful tuning of the device parameters such as $\Phi_{M2}$, $\varepsilon_{ox2}$, NJD, and $L_C$. The work thus presents a GEWE-RC MOSFET design as a promising solution for realizing CMOS technology for high-performance applications where device reliability is a major concern.

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REFERENCES

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