Gate dielectric engineering of quarter sub micron AlGaN/GaN MISHFET: A new device architecture for improved transconductance and high cut-off frequency

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1. Introduction

The gallium nitride (GaN) and its related alloys based semiconductor materials have been attracting attention because of their large bandgap and their ability to operate at high power, high temperature and high speed. Such qualities have led to investigation of these material systems for various devices including metal insulator semiconductor heterostructure field effect transistors (MISFETs), HFETs, heterojunction bipolar transistors (HBTs), metal oxide semiconductor field effect transistors (MOSFETs), photodetectors, and photodetectors. Tremendous commercial applications await any successful and desirable demonstration of these devices. Radio frequency (RF) power amplification is one example where AlGaN/GaN HFETs are sought after [1,2]. However, large gate leakage currents and inferior noise characteristics of AlGaN/GaN HFETs led to the development of AlGaN/GaN based MISHFET structure. The AlGaN/GaN MISHFET is characterized by a thin gate dielectric and has received much attention recently due to its capability to combine the advantages of dielectric layer and AlGaN/GaN hetero-structure. The MISHFET approach allows for application of high positive gate voltages to further increase the sheet carrier density in the 2-DEG channel and hence the device peak currents [3–6]. It has demonstrated excellent electrical performance and applications such as high frequency wireless base stations, broad band links, etc. Commercial and military radar and satellite communication could benefit from such a device. However, there are many milestones to be achieved and the work in this field is far from complete. In order to achieve superior RF performance for high frequency applications, short gate length is required for compound field effect transistors. The gain and noise characteristics of the MISHFETs at high frequency are strongly dependent on the gate length and the gate resistance values. Several gate dielectric engineered structures like T-gate, Γ-gate [7] etc. are currently being used for reliability improvement for low noise and high gain characteristics. T-shaped gate structures are most extensively studied as they are characterized by small foot which defines the small gate length and the wide top which provides a low gate resistance [8]. Different lithography methods have been developed for the submicrometer T-gates in recent years [9,10]. For example, multi-layer photo resist processes have been used to obtain submicrometer T-shaped gates [11]. In order to further improve device performance, dielectric deposition process with etching back technology have been widely used to form dielectric sidewall and shrink the gate length that is originally limited by the lithography resolution [12]. The thermally reflowed resist process is another approach for gate shrinkage and has been reported by Meng and
Lee et al [13–14]. Tightly controlled process and relatively complicated steps are required for these processes. However, challenges posed by fundamental limits have led to the continuous exploration of new device structures for the technological progression of semiconductor industry. Therefore to utilize the combined advantages of both T-shaped structure and AlGaN/GaN MISHFET, we for the first time have theoretically proposed the gate dielectric engineering for AlGaN/GaN MISHFET structure and systematically examined its effect on electrical characteristics of the proposed device. Different combinations of dielectrics like SiO2, Si3N4 have been investigated. A closed form expression for drain current has been formulated by taking into account the highly dominant effect of spontaneous and piezoelectric polarization at the AlGaN/GaN interface. The proposed model includes $E_l$ as a function of $n_t$ by a simple polynomial in the $n_t - V_{gs}$ expression and account for the whole range of operation i.e. from subthreshold to deep saturation region. The proposed analysis can also predict the performance of HFETs by adjusting few parameters. The effects of parasitic source drain resistances and velocity saturation have also been included to accurately develop the dc model. To generalize the model, the pulse doped structure comprising the Schottky cap layer, dopant layer and spacer layer is employed. Other relevant parameters like threshold voltage, 2-DEG (two dimensional electron gas) density, transconductance and cut-off frequency have also been examined. Results are validated by available experimental data [6]. The new gate engineered MISHFET exhibits high transconductance and improved cut-off frequency.

2. Model formulation

The basic schematic structure used in the analysis alongwith proposed gate dielectric schemes is shown in Fig. 1. It consists of SiC substrate, an undoped GaN layer to form 2-DEG channel, an undoped AlGaN spacer layer of thickness $d_i$, a n-doped AlGaN layer of thickness $d_d$ to provide 2-DEG and an undoped AlGaN cap layer of thickness $d_c$. To study the effect of position of dielectric and their thicknesses, the region between gate and the high band gap semiconductor viz. AlGaN is divided into three identical rectangular regions. Poisson’s equation is then solved separately for each identical rectangular region to maintain the continuity of current flow amongst the three regions. Each region has dimensions $L_g/3 \times t_{ox}$ where $L_g$ is the normal gate length and $t_{ox}$ is the thickness of the dielectric and is characterized by electric permittivity $\varepsilon_{ox}$

\[ n_{ox}(x) = \frac{\beta}{d(d_i + x)} [V_{gs} - V_{thz} - E_l] \]

And respective threshold voltage for each region can be expressed as:

\[ V_{thz} = \phi_b(m) - \Delta \phi_s - \frac{qN_d d_i^2}{2\beta} \left(1 + \frac{2d_i}{d_d}\right) \frac{qN_d x_i d_d}{\varepsilon_{ox} t_{ox}} - \frac{\sigma_{ox}(m)(d_i + x)}{\beta} + k_1 \]

where $z = 1, 2, 3$ for regions I, II and III, respectively. These three rectangular structures are then analyzed for different combinations of two different dielectrics viz. Si3N4 and SiO2 as given in Table 1. These gate dielectric schemes are then broadly categorized into T and $\Gamma$ shaped schemes based on performance resemblance to T and $\Gamma$ gate HFET structures. They are then compared with the uniform schemes for both dielectrics. For current conduction through the device, the current should flow through all the three regions consistently. Hence the actual threshold voltage of the device is determined by the lowest threshold voltage amongst the three regions. The electrical characteristics of scheme A are similar to schemes B and C. Analogous is the case for scheme D with schemes E and F. The expression for 2-DEG sheet carrier density is calculated region-wise as in [15, 18] and is as follows:

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Table 1: Region-wise distribution of gate dielectric permittivities

<table>
<thead>
<tr>
<th>Region</th>
<th>Region I</th>
<th>Region II</th>
<th>Region III</th>
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<tbody>
<tr>
<td>A</td>
<td>SiO2</td>
<td>Si3N4</td>
<td>SiO2</td>
</tr>
<tr>
<td>B</td>
<td>Si3N4</td>
<td>SiO2</td>
<td>SiO2</td>
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<tr>
<td>C</td>
<td>SiO2</td>
<td>SiO2</td>
<td>Si3N4</td>
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<tr>
<td>D</td>
<td>Si3N4</td>
<td>Si3N4</td>
<td>SiO2</td>
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<td>E</td>
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<td>Si3N4</td>
<td>Si3N4</td>
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<tr>
<td>F</td>
<td>Si3N4</td>
<td>SiO2</td>
<td>Si3N4</td>
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<td>G</td>
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<td>Si3N4</td>
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<td>H</td>
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the dopant layer and $E_t$ is the position of fermi level with respect to the bottom of the conduction band in GaN (as given in Table 2).

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$\sigma_{ps}(m) = \frac{2}{a(m)} \left( e_{31}(m) - e_{33}(m) \frac{C_{33}(m)}{C_{13}(m)} + P_{sp}(0) - P_{sp}(m) \right)$

where $a(m)$ is the lattice constant, $e_{31}(m)$ and $e_{33}(m)$ are piezoelectric constants, $C_{33}(m)$ and $C_{13}(m)$ are elastic constants and $P_{sp}(m)$ is the spontaneous polarization.

Though the assumption of linear approximation of $E_t$ Vs $n_a$, and $E_t$ = 0 lead to simple expressions for $n_i(x)$, the results are valid for a very small range of device operation. In our model, we represent $E_t$ as a non linear function of $n_i(x)$ by the simple polynomial expression which is valid for entire range of operation i.e. from subthreshold to saturation region:

$E_t = \frac{k_1 + k_2 \sqrt{n_i} + k_3 n_i}{a}$

The values of $k_1$, $k_2$, and $k_3$

$k_1 = -0.1794$ $V \quad k_2 = 2.991 \times 10^{-3}$ $V m$

$k_3 = -0.657 \times 10^{-18}$ $V m^2$

were obtained using the effective mass of electron (0.22 $m_e$) for AlGaN/GaN system following the same approach as proposed by Nandita and Amitava Dasgupta et al. [17].

### 2.1. $I_d$-$V_d$ characteristics

The drain current for each region is evaluated using the following expression:

$I_{dz2} = qWn_{inz}(x)V(x)$

where $q$ is the electronic charge, $w$ is gate width and $x$ is any arbitrary position along the channel. For analytical simplicity the following velocity field relation is used:

$V(x) = \frac{\mu E(x)}{1 + E(x)/E_c}$ for $E \leq E_c$ \hspace{1cm} (6a)

$v_{sat} \quad$ for $E > E_c$ \hspace{1cm} (6b)

where $\mu$ is mobility of electron, $E_c = v_{sat}/\mu$ is critical field due to velocity saturation, $v_{sat}$ is the saturation velocity.

To calculate $I_{dz}$, we substitute $n_{inz}$ and $V_{thz}$ from (1) and (2), we get:

$I_{dz} = \frac{q^2(d_1 + x)^2}\mu w -16\beta(q(d_1 + x) + \beta k_3)\left( \frac{f_{1}(y_{12}) - f_{1}(y_{in})}{(l + (\mu V_{12} - V_{thz})v_{sat})} \right)$

where

$f_{1}(y) = \left( \frac{5k_2}{q(d_1 + x)} \right)^2 \frac{y}{2} \frac{y^2}{3(q(d_1 + x))}$

$y_{12} = \left( \frac{5k_2}{q(d_1 + x)} \right)^2 \frac{y}{2} \frac{y^2}{3(q(d_1 + x))} \left( 1 + \frac{\beta k_3}{q(d_1 + x)} \right)$

$y_{inz} = \left( \frac{5k_2}{q(d_1 + x)} \right)^2 \frac{y}{2} \frac{y^2}{3(q(d_1 + x))} \left( 1 + \frac{\beta k_3}{q(d_1 + x)} \right)$

### 2.2. Transconductance

For the optimization of FETs in high frequency applications, the transconductance ($g_m$) plays a significant role. It is one of the most important indicators of device quality for microwave applications and is evaluated as:

$g_m = \frac{\partial I_d}{\partial V_{gs}} |_{V_{ds}=const}$

where $g_m$ is given as the ratio of transconductance $g_{inz}$ to the total gate capacitance $C_{gr}$ i.e.

$g_m = \frac{g_{inz}}{2\pi C_{gr}}$ \hspace{1cm} (10)

And is written by substituting the value of $g_{inz}$ from (9) and $C_{gr}$ is calculated by the parallel combination of insulator capacitance $C_{inz}$ and bulk capacitance $C_b$ as follows:

$C_{gr} = \sum_{i=1}^{3} \frac{C_{inz}C_b}{C_{inz} + C_b}$ \hspace{1cm} (11)

where $C_b = \frac{\alpha w a_{inz}}{E_{inz}}$, $C_{inz} = \frac{\alpha w a_{inz}}{E_{inz}}$ and $w a_{gr}/3$ denotes the effective area under each gate region. The transconductance and cut-off frequency are calculated for the entire range of operation viz subthreshold to saturation region.

### 3. Results and discussion

An analytical model has been presented to study the dc current voltage characteristics and small signal microwave parameters of gate dielectric engineered AlGaN/GaN MISHFET. The parameters used for the study are listed in Table 2. To explore the performance of the FET, the drain current for each region is evaluated using the follow-
enhancements of MISHFET and to prove the validity of the proposed model, the results are compared with conventional MISHFET structures and experimental data, respectively.

The variation for transconductance with gate voltage for various gate dielectric schemes is shown in Fig. 2. A high transconductance of 170 mS/mm is obtained for T-shaped geometry as compared to 130 mS/mm of Γ-shape. Minimum transconductance of 77 mS/mm is obtained for uniform SiO₂ dielectric distribution. High transconductance implies high dc amplification offered by T-shaped MISHFET. Inset shows the analogous comparison of transconductance for T- and Γ-gate HFET structures with uniform gate HFET structure.

Transfer curves for all schemes are shown in Fig. 3. To validate the model, variation of drain current with gate voltage for uniform SiO₂ and Si₃N₄ profiles (indicated by hollow symbols viz. □-Si₃N₄, △-SiO₂) are compared with experimental data (corresponding filled symbols) [6] in the inset of Fig. 3 and show excellent agreement. This variation occurs because the region having Si₃N₄ as dielectric has high threshold voltage in comparison to the region having SiO₂.

Both the threshold voltage and drain current are scaled with respect to gate dielectric thickness as seen in Figs. 4 and 5, respectively. These results confirm that no hidden parameters obscure the scaling behaviour and it primarily depends on $t_{in}$.
Fig. 6 shows the variation of transconductance-to-drain current ratio with gate dielectric thickness for all gate dielectric schemes at a gate length of 1 μm. Lower values of dielectric thickness are extremely important to realize higher values of $g_m/I_d$. A careful selection of $t_m$ is thus required as it governs the transconductance generation efficiency of the device.

Fig. 7 clearly shows that the introduction of gate dielectric schemes leads to increase in maximum cut-off frequency from 8 GHz for uniform dielectric scheme to 9 GHz for Γ-gate to 10.5 GHz for T-gate scheme.

4. Conclusion

The novel gate dielectric engineered AlGaN/GaN MISHFET structure has been analyzed and its performance comparison with uniform gate dielectric structure is discussed. Study reveals that these gate dielectric schemes offer superior characteristics in terms of high transconductance and cut-off frequency, which further result in enhanced speed and power performance of the device. Gate dielectric schemes A, B and C resembles the performance enhancements as that obtained by using T-gate HFET structures. Similarly with gate dielectric schemes D, E and F a boost in rf performance metrics are achieved as that for Γ-gate HFET structures. Improvements on device microwave performance for various gate dielectric schemes over conventional MISHFET structures as shown in Figs. 2 and 7 have been observed analogous to the benefits of T- and Γ-gate HFET structures over conventional HFET structures. Hence, by using this model similar effects as in case of T-gate or Γ-gate HFET structures can also be created which can predict accurate technological details of device even prior to the fabrication.

T-shaped gate dielectric scheme shows best performance as expected amongst all the three types of structures with highest cut-off frequency of 10.5 GHz. The proposed modeling scheme is capable of predicting the microwave characteristics of uniform gate dielectric MISHFETs and even HFETs as explained in Table 1, by altering $v_{max}$ or the value of $t_m$ in the model. These gate dielectric schemes allow greater flexibility than uniform dielectric structures in selecting device parameters for performance prediction, device optimization and design that are extremely important for circuit realization. Gate dielectric engineering is thus a suitable alternative for short gate length MISHFETs where limitations of lithographic tools prevent further scaling.

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References