Two-dimensional analytical subthreshold model of graded channel DG FD SOI n-MOSFET with gate misalignment effect

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ABSTRACT

A two-dimensional (2-D) analytical subthreshold model is developed for a graded channel double gate (DG) fully depleted SOI n-MOSFET incorporating a gate misalignment effect. The conformal mapping transformation (CMT) approach has been used to provide an accurate prediction of the surface potential, electric field, threshold voltage and subthreshold behavior of the device, considering the gate misalignment effect to be on both source and drain side. The model is applied to both uniformly doped (UD) and graded channel (GC) DG MOSFETs. The results of an analytical model agree well with 3-D simulated data obtained by ATLAS-3D device simulation software.

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1. Introduction

DG-SOI is a promising CMOS device to be scaled beyond the 100-nm regime [1], as it exhibits an almost ideal sub-threshold swing (S ≈ 60 mV/dec), lower output conductance and higher drive current for analog applications [2]. One major issue of DG-MOSFETs is the alignment between the top and bottom gates. There are some self-aligned DG-MOSFETs proposed in the literature [3,4], however, complicated fabrication techniques are usually required. It would then be critical to understand how the misalignment between the gates would affect the properties of DG-MOSFETs, especially the SCE’s, subthreshold slope and device performance.

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Fig. 1. Schematic structure of GC DG FD SOI MOSFET with gate misalignment of $m_a$ for $L = 60$ nm, $L_1:L_2 = 1:1$, $t_{Si} = 10$ nm, $t_{ox1} = t_{ox2} = 2$ nm.

Fabrication of planar DG-SOI in the sub-100 nm regime with an ideal self-aligned structure is very difficult. The tolerance range of the gate misalignment value must be carefully studied and experimentally verified. Gate misalignment produces S/D asymmetric effects. We shall analyze the S/D asymmetric effect caused by gate nonoverlapping. The gate nonoverlapped region introduces extra series resistance and a weakly controlled channel, which will degrade the SCE of the device. As a result the drain potential can easily extend towards the channels through the bottom part of the channel region. Part of the applied $V_{DS}$ is dropped on the additional series resistance, so the effective $V_{DS}$ applied on the channel region was actually reduced. The impact of gate misalignment is also significant for $I_{on}$ in DG MOSFETs. A large back gate (BG) shift towards source reduces the on current ($I_{on}$) compared with the aligned case, whereas a slight BG shift increases the $I_{on}$. This is due to a lower source access resistance. In terms of short channel effects, aligned transistors exhibit the best control while highly misaligned MOSFETs operate like single gate ones. $I_{off}$ is much more influenced by the misalignment than $I_{on}$ due to a degradation of the electrostatic control.

Although significant progress has been made over the past few years, additional development work in terms of modeling/simulation of device parameters is required for GC MOSFETs to aid in technology development, device structure optimization, and advanced design. Furthermore, a GC device has not been analyzed so far and the research on UD DG devices has mainly focused on short channel effects and charge control [5,6]. Recently, “laterally asymmetric channel” devices also known as Graded Channel (GC) DG-MOSFET have been reported [7–10], to overcome problems such as (a) hot electron degradation, (b) threshold voltage roll-off and (c) parasitic bipolar effects, exhibited by uniformly doped (UD) DG devices. The GC SOI MOSFET is an asymmetric channel device, which was initially introduced to minimize bipolar effects in FD transistors [11]. An undoped (i.e. low doped) region of length $L_{LD}$ is preserved at the drain side of the channel. This low doped region presents a low threshold voltage as compared with the high doped region of length $L_{HD} = L - L_{LD}$ (where $L$ is the total channel length) close to the source as shown in Fig. 1. The doping level at the source side is higher than at the drain, reducing the electric field near the drain end and total amount of carriers generated by impact ionization.

Highly accurate and physics-based compact models, which are at the same time computationally efficient, are required for proper modeling of MOSFETs for VLSI circuit simulation. Existing surface potential-based models generally rely on numerical iteration to solve their fundamental equations.
Still, explicit analytical models are highly desirable because they offer better computational efficiency than their numerical alternatives without loss of physical insight. We have presented a two dimensional closed form analytical model of a graded channel (GC) DG-SOI MOSFET, considering the misalignment of the bottom gate on both source (DGS) and drain (DGD) sides. The model uses a conformal mapping transformation approach to include the fringing field effect arising at the bottom gate electrode in the ungated region, which can provide an accurate prediction of the subthreshold behavior of the device. The results so obtained have been verified with the ATLAS 3-D device simulator.

1.1. Model formulation

A graded channel (GC) DG-SOI n-MOSFET with gate misalignment (m_g) is shown in Fig. 1. In this structure n⁺ top and bottom poly-silicon gates (N_poly = 1.65 × 10^{25} m^{-3}), top gate oxide as (t_{ox1} = 2 nm), bottom gate oxide as (t_{ox2} = 2 nm), silicon film thickness as (t_{Si} = 10 nm), p-type channel impurity concentration in the high and low doped regions as N_1 and N_2, with the lengths as L_1 and L_2 respectively. The 2-D Potential distribution can be obtained by solving 2-D Poisson equation.

\[ \nabla^2 \psi (x, y) = \frac{qN_i}{\varepsilon_{Si}} \]

where \( i = 1 \) and \( 2 \) for the highly doped and lightly doped regions respectively. In order to simplify the analysis, the polysilicon depletion effect [12–14] and the quantum effect [15–17] are not considered.

The thin film is divided into three regions:
- **Case I:** Gate overlap highly doped region
- **Case II:** Gate overlap lightly doped region
- **Case III:** Non-gate overlap lightly doped region

**Case I:** Gate overlap highly doped region.

The potential profile in the vertical direction \( \psi (x, y) \) can be approximated by a 2-D parabolic approximation.

\[ \psi_i(x, y) = C_{bi}(y) + C_{Si}(y)x + C_{2i}(y)x^2. \]  

Solving 2-D Poisson’s equation with these boundary conditions

\[ \left. -\frac{\partial \psi_i(x, y)}{\partial x} \right|_{x=0} = \frac{C_{ox2}}{\varepsilon_{Si}} [V_G + \phi_f(x) - \psi_{bi}(y)], \quad \left. -\frac{\partial \psi_i(x, y)}{\partial x} \right|_{x=t_{Si}} = \frac{C_{ox1}}{\varepsilon_{Si}} [\psi_i(y) - V_G - \phi_f]. \]

\[ \psi_i(x, y) = \psi_{bi}(y) - \frac{\varepsilon_{ox}}{\varepsilon_{Si} t_{ox2}} \left[ V_G + \phi_f - \psi_{bi}(y) \right] \]

\[ + \frac{1}{t_{ox2}} \left[ \left( t_{ox2} + \frac{\varepsilon_{ox} t_{Si}}{\varepsilon_{Si} t_{ox2}} + t_{ox1} \right) (V_G - \psi_{bi}(y)) + \left( t_{ox1} + \frac{\varepsilon_{ox} t_{Si}}{\varepsilon_{Si} t_{ox1}} \right) \phi_f \right] + \phi_f. \]  

Using Eqs. (2)–(3), a relationship between front and back surface potentials has been obtained as

\[ \psi_{Si}(y) = \psi_{bi}(y) - \frac{\varepsilon_{ox} t_{Si}}{\varepsilon_{Si} t_{ox2}} [V_G + \phi_f - \psi_{bi}(y)] + P_{21}(y) t_{Si}^2. \]  

Assuming silicon film to be very thin (\( t_{Si} \approx 10 \text{ nm} \)), we can write

\[ \frac{\partial^2 \psi_i(y)}{\partial y^2} \approx \frac{1}{k_{Si}} \frac{\partial^2 \psi_{bi}(y)}{\partial y^2} \]

where \( k_{Si} \) is the parameter that accounts for the correlation between the derivative of the lateral electric field at any depth in the thin film and the derivative of the lateral electric field at the back.
Si–SiO\(_2\) surface [18,19]. From Eqs. (1), (2) and (5) with the coefficients given in Table 1, the differential equation in terms of back surface potential can be written as:

\[
\frac{d^2 \psi_{\text{bi}}(y)}{dy^2} - \frac{2\varepsilon_{\text{ox}}}{\varepsilon_{\text{Si}}} \left( \frac{t_{\text{ox2}}}{t_{\text{Si}}} + \frac{t_{\text{ox}}}{t_{\text{Si}}} + t_{\text{ox1}} \right) \psi_{\text{bi}}(y) = \frac{qN_i}{\varepsilon_{\text{Si}}} \left[ \frac{2\varepsilon_{\text{ox}}}{\varepsilon_{\text{Si}}} \left( \frac{t_{\text{ox2}}}{t_{\text{Si}}} \right) + 2\varepsilon_{\text{ox}} \right] \left( V_G + \left( \frac{t_{\text{ox1}}}{t_{\text{Si}}} \right) \phi_2 + 2\phi_1 \right). 
\]

(6)

Solving this, the back surface potential is given as

\[
\psi_{\text{bi}}(y) = V_{\text{bi}} e^{\sqrt{2\varepsilon_{\text{ox}}}y} + V_{\text{bi}} e^{-\sqrt{2\varepsilon_{\text{ox}}}y} - \frac{A_{\text{bi}}}{A_{\text{qi}}}
\]

(7)

where

\[
A_{\text{bi}} = \kappa_{\text{Si}} \frac{qN_i}{\varepsilon_{\text{Si}}} \left( \frac{2\varepsilon_{\text{ox}}}{\varepsilon_{\text{Si}}} \left( \frac{t_{\text{ox2}}}{t_{\text{Si}}} \right) + 2\varepsilon_{\text{ox}} \right), \quad A_{\text{qi}} = \frac{2\varepsilon_{\text{ox}}}{\varepsilon_{\text{Si}}} \frac{t_{\text{ox1}}}{t_{\text{Si}}}.
\]

\[
t_1 = t_{\text{ox1}} + \frac{\varepsilon_{\text{ox}}}{\varepsilon_{\text{Si}}}, \quad t_2 = 1 + \frac{2\varepsilon_{\text{ox}}}{\varepsilon_{\text{ox}}}, \quad t_3 = t_{\text{ox2}} + \frac{\varepsilon_{\text{ox}}}{\varepsilon_{\text{Si}}}, \quad t_{\text{ox1}}.
\]

V_{\text{bi}}, V_{\text{qi}} are the coefficients to be determined in Appendix.

Solving Eq. (5) with the coefficient (C2), the front surface potential \(\psi_{\text{Si}}(y)\) in terms of back surface potential \(\psi_{\text{bi}}(y)\) in the gate overlap region can be written as

\[
\psi_{\text{Si}}(y) = \frac{1}{t_{\text{ox2}}} \left[ \sigma_1 \left( 1 + \frac{2\varepsilon_{\text{Si}}}{\varepsilon_{\text{ox}}} + \frac{t_{\text{ox1}}}{t_{\text{ox2}}} \right) \psi_{\text{bi}}(y) + \left( \frac{t_{\text{ox2}}}{t_{\text{ox1}}} - 1 \right) V_G - \phi_1 \right] + \frac{\phi_1}{t_{\text{ox1}}}. 
\]

(8)

From Eqs. (7) and (8), we get the front surface potential as

\[
\psi_{\text{Si}}(y) = V_{\text{si}} e^{\sqrt{2\varepsilon_{\text{ox}}}y} + V_{\text{ri}} e^{-\sqrt{2\varepsilon_{\text{ox}}}y} - D_{\text{i}}
\]

(9a)

where

\[
D_{\text{i}} = \frac{1}{t_{\text{ox2}}} \left[ \sigma_1 \frac{t_{\text{ox1}}}{t_{\text{ox2}}} \psi_{\text{bi}}(y) + \left( 1 - \frac{t_{\text{ox1}}}{t_{\text{ox2}}} \right) V_G + \phi_1 \right] - \frac{\phi_1}{t_{\text{ox1}}}. 
\]

(9b)

\(V_{\text{si}}, V_{\text{ri}}\) are the coefficients to be determined in Appendix. \(\sigma_1 = 0.94 - 2m_a \times 10^2\) is an empirical correction factor to account for the symmetric structure in the gate overlap region, \(m_a\) is the gate misalignment as shown in Fig. 1.
Case III: Non-gate overlap lightly doped region

The electrostatic potential in the non-gate overlap region could be written as in the gate overlap region:

\[ \psi_3(x, y) = C_{03}(y) + C_{13}(y)x + C_{23}(y)x^2. \]  

(10)

Using Eq. (10) with the boundary conditions

\[ -\frac{\partial \psi_3(x, y)}{\partial x} \bigg|_{x=0} = \frac{\varepsilon_{ox}}{\varepsilon_{Si} t(y)} [V_G + \phi_{f2} - \psi_{b3}(y)], \quad -\frac{\partial \psi_3(x, y)}{\partial x} \bigg|_{x=t_i} = \frac{C_{ox1}}{\varepsilon_{Si}} [\psi_{s3}(y) - V_G - \phi_{f1}] \]

\[ \psi_{s3}(y) = \psi_{b3}(y) - \frac{\varepsilon_{ox}}{\varepsilon_{Si} t(y)} [V_G + \phi_{f2} - \psi_{b3}(y)] t_i + C_{23}(y)t_i^2 \]  

(11)

where, the coefficients used in the above equation are given in Table 1, \( t(y) \) is the distance from the right edge of the bottom gate to the back surface channel. Using a similar approximation approach as for the gate overlap region (I), we can write:

\[ \frac{\partial^2 \psi_3(y)}{\partial y^2} \approx \frac{1}{\kappa_{S2}} \frac{\partial^2 \psi_{b3}(y)}{\partial y^2}. \]  

(12)

From (1) and (10), back surface potential for the lightly doped non gate overlap region is given as

\[ \frac{\partial^2 \psi_{b3}(y)}{\partial y^2} = \kappa_{S2} \left[ \frac{\partial^2 \psi_3(y)}{\partial y^2} \right] = \kappa_{S2} \left[ \frac{qN_2}{\varepsilon_{Si}} - 2C_{23}(y) \right]. \]  

(13)

To simplify the analysis, a conformal mapping transformation approach has been used [20]. Using this approach, we can transform the original \( xX + yY \) space in terms of \( X \) and \( Y \) axes to the \( uU + vV \) space in terms of \( U \) and \( V \) axes based on the following transfer function:

\[ (y - L_m)\bar{Y} + nxx = k \sinh(uU + vV) \]

\[ L_m = L_c - m_a \]

\[ n = \frac{m_a}{t_{ox2} \sinh \left[ \cosh^{-1} \left( \frac{t_{ox2} + f_{ox2}}{t_{ox2}} \right) \right]}, \quad k = \frac{m_a}{\sinh \left[ \cosh^{-1} \left( \frac{t_{ox2} + f_{ox2}}{t_{ox2}} \right) \right]} \]

From the above formula, \( xX + yY \) coordinates are transformed into \( uU + vV \) coordinates. As a result, the arc-shaped electric field contour in the ungated region has become straight line shaped.

The back surface potential is obtained as

\[ \psi_{b3}(y) = j_1 e^{\frac{y}{\gamma} - L_m} + j_2 e^{-\frac{y}{\gamma} - L_m} + \frac{B_1}{B_0} \]

(14)

where

\[ k = \frac{m_a}{\sinh \left[ \cosh^{-1} \left( \frac{t_{ox2} + f_{ox2}}{t_{ox2}} \right) \right]}, \quad \gamma = \sqrt{-B_0}, \]

\[ B_0 = 2\kappa_{S2}k^2\alpha_0, \quad B_1 = \kappa_{S2}k^2 \left[ \frac{qN_2}{\varepsilon_{Si}} - 2\beta_0 \right] \]

\( j_1 \) and \( j_2 \) are the coefficients to be determined in Appendix.

The front surface potential \( \psi_{s3}(y) \) and back surface potential \( \psi_{b3}(y) \) are correlated as

\[ \psi_{s3}(y) = \frac{1}{t(y)} \left[ \sigma_2 \left( 1 + \frac{2\varepsilon_{ox} t(y)}{\varepsilon_{Si} t_{ox1}} \right) \psi_{b3}(y) + \left( \frac{t(y)}{t_{ox1}} - 1 \right) V_G - \phi_{f2} \right] + \frac{\phi_{f1}}{t_{ox1}}. \]  

(15)
Substituting, Eq. (14) in (15), we find

\[ \psi_{G3}(y) = j_3 e^{-\frac{\psi}{t}(y-l_m)} + j_4 e^{-\frac{\psi}{t}(y-l_m)} + D_3 \]  

(16a)

where

\[ D_3 = \frac{1}{t(y)} \left[ \frac{\sigma_2 t_6 \beta_1}{\varepsilon_{ox}} + t_4 V_G - \phi_f/2 \right] + \frac{\phi_{f1}}{t_{ox}} \]  

(16b)

\[ t_4 = 1 - \frac{t(y)}{t_{ox}}, \quad t_5 = \frac{1}{t_{ox}} + \frac{2\varepsilon_{Si}}{\varepsilon_{ox} \varepsilon_{Si}}, \quad t_6 = 1 + \frac{2\varepsilon_{Si} t(y)}{\varepsilon_{ox} \varepsilon_{Si}} \]  

(16c)

\[ \sigma_2 = 0.51 + 4m_a \times 10^2 \] is an empirical factor to account for the non-symmetric structure in the non-gate overlap region. \( j_3 \) and \( j_4 \) are the coefficients to be determined in Appendix.

1.2. Subthreshold analysis

Knowing the potential solution, the current density (both drift and diffusion) [21,22] can be written as

\[ J = -q \mu n(x, y) \frac{d\phi_n(y)}{dy}. \]  

(17)

Integrating Eq. (17), we get

\[ I_{ds}(y) = -\mu W \frac{d\phi_n(y)}{dy} Q_s(y). \]  

(18)

Where, \( Q_s(y) = \int_0^{Si} n(x, y) dx = \int_0^{Si} n_i e^{[\psi_S(x,y) - \phi(\psi_S(y))]/kT} dx \) is the inversion charge per unit gate area and \( \psi_S(x,y) \) is the total surface potential.

The integration of Eq. (18) from 0 to \( L \) yields:

\[ I_{ds}(y) = \mu W \int_0^{V_{ds}} e^{-\phi_n(y)/kT} dy. \]  

(19)

Hence, the subthreshold current expression for GC DG–FD SOI n-MOSFET can be expressed as

\[ I_{ds}(y) = \mu W \int_0^{V_{ds}} e^{-\phi_n(y)/kT} dy \int_0^{l_m/2} dt \int_0^{l_m/2} dy + \int_0^{l_m} dy + \int_0^{l_m} dy \]  

(20)

which is a unified solution and can be used to calculate the subthreshold current for UD & GC channel DG SOI for different gate misalignments.

2. Results and discussion

In all figures the symbols represent the simulated data and the lines represent the analytical results. The simulated results were obtained using ATLAS 3-D device simulator incorporating the concentration dependent mobility model and electric field dependent carrier mobility model with velocity saturation. The various UD and GC DG devices analyzed in our work are given in Table 2, which shows the effect of gate misalignment on various device parameters such as threshold voltage, DIBL and subthreshold slope for both DGD and DGS configurations. The threshold voltage was defined as the gate voltage at \( 10^{-7} \) A/\( \mu \)m drain current in order to estimate \( I_{\text{off}} \) current; DIBL has been calculated as differences of threshold voltage at \( V_{DS} = 50 \) mV & 1.0 V; Subthreshold Slope is defined as the change in gate voltage \( V_{GS} \) required to reduce the subthreshold current \( I_{DS} \) by one decade and extracted at \( V_{DS} = 50 \) mV. Fig. 2 shows the variation of subthreshold slope with gate misalignment...
for the UD and the GC DG (n⁺/n⁺ and the n⁺/p⁺) SOI MOSFET. From Fig. 2(a), the subthreshold slope for zero gate misalignment case (m₀ = 0), is found to be 63.29 mV/decade (Table 2(a)). As we increase the misalignment by m₀ = 5 nm, the subthreshold slope increases by 0.27% and 0.35% for the DGD and the DGS configurations respectively. These values increase by 1.28% and 1.79% with the increase in misalignment by m₀ = 15 nm. This shows a larger effect of gate misalignment for the DGS structure in comparison with the DGD structure. This is due to the reduction in the fringing field effect that arises at the source side in the absence of drain voltage. For the GC architecture, the subthreshold slope for zero gate misalignment case (m₀ = 0), is found to be 63.09 mV/decade. As we increases the misalignment by m₀ = 5 nm, the subthreshold slope increase by 0% and 1.03% for the DGD and the DGS configurations respectively. These values increase by 0.63% and 3.17% with the increase in misalignment by m₀ = 15 nm. This shows that GC architecture having a high-low doping profile demonstrates a lesser effect of gate misalignment for the DGD configuration in comparison with the UD DG devices while it shows a larger effect of gate misalignment for the DGS structure in comparison with the UD DG devices. This is because misalignment occurs in the highly doped region for the DGS configuration of GC architecture, which controls the device characteristics. Fig. 2(b) shows the variation of subthreshold slope with gate misalignment for the UD and GC asymmetrical DG (n⁺/p⁺) SOI MOSFET. While comparing it with symmetrical DG (n⁺/n⁺) SOI MOSFET, it is found that symmetrical DG provides better immunity to the effects of gate misalignment in comparison with the asymmetrical DG for both the UD and GC architectures (Table 2). This is because in symmetrical DG devices, both the gates control the channel with the same strength but in the asymmetrical DG structure, the n⁺ gate controls the channel more effectively than the p⁺ gate. Therefore if the bottom gate is misaligned in the (n⁺/p⁺) DG MOSFET, the barrier between the source and channel due to the drain voltage becomes effectively lower as compared with the (n⁺/n⁺) case, so the drain current increases and thus, the threshold voltage decreases. In contrast the threshold voltage of the (n⁺/n⁺) DG MOS increases as the misalignment of the bottom gate increases. This can be also be seen through the variation of the back surface potential along the channel (Figs. 3 and 4), and transmission of misalignment effect to the front gate has been studied through the variation of front surface potential along the channel (Fig. 5). The threshold voltage of the device is controlled by the minima of the channel potential and for a symmetrical double gate device; the minimum surface potential decreases with increase in misalignment thereby increasing the threshold voltage of the device as shown in Fig. 3. For an asymmetrical DG device, the minimum surface potential increases with increase in misalignment thus reducing the threshold voltage of the device as shown in Fig. 4. The analytical results are compared with simulated results to validate our model.

Fig. 2. (a), (b) Subthreshold slope variation with gate misalignment for UD & GC DG SOI for VDS = 50 mV, L = 60 nm, t-navigation = 10 nm, tox1 = tox2 = 2 nm (a) Symmetrical DG (n⁺/n⁺) SOI (b) Asymmetrical DG (n⁺/p⁺) SOI.
Table 2
Device parameters of UD and GC DG devices analyzed in the present work for different gate misalignment for $L = 60$ nm, $t_{Si} = 10$ nm, $t_{ox1} = t_{ox2} = 2$ nm (a) Symmetrical DG ($n^+ / n^+$) device (b) Asymmetrical DG ($n^+ / p^+$) device.

<table>
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<th>Doping (cm$^{-3}$)</th>
<th>$m_a$ (nm)</th>
<th>Vth (V)</th>
<th>DIBL</th>
<th>Subthreshold slope</th>
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<td>0.1580</td>
<td>0.1640</td>
<td>10.63</td>
</tr>
<tr>
<td>N$_A$ = 1 x 10$^{18}$</td>
<td>DGS 10</td>
<td>0.1632</td>
<td>0.1655</td>
<td>8.69</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>0.1609</td>
<td>0.1570</td>
<td>9.27</td>
</tr>
<tr>
<td>N$_2$ = 1 x 10$^{18}$</td>
<td>DGS 15</td>
<td>0.1533</td>
<td>0.1481</td>
<td>10.09</td>
</tr>
</tbody>
</table>

and low doped regions as compared with the UD devices that demonstrates a lesser effect of gate misalignment for the GC devices in comparison with the UD DG devices. Further, the minimum surface potential increases as we go from UD to GC devices, thereby reducing the electric field near the drain and the total amount of carriers generated by impact ionization and is shown in Fig. 3(c)–(d). As shown in Figs. 4 and 5 the analytical model considering the fringing electric field effect could predict front and back surface potential distribution consistently and results obtained are verified with the 3-D simulation results. This shows that in case of front surface potential the effect of gate misalignment is less in comparison with the back surface potential due to larger fringing field effect at the back surface. The dip in the back surface potential is less in comparison with the front surface. As the gate misalignment increases, the location of the minimum back surface potential moves toward the drain end and is shown in Fig. 4.

Figs. 6 and 7 shows the variation of subthreshold current with gate bias for $V_{DS} = 50$ mV for different channel doping concentrations for the UD & GC DG devices. The subthreshold characteristics always become worse as the misalignment increases. It is because the total gate capacitance in comparison with the drain capacitance decreases as the misalignment increases resulting in deterioration of channel controllability. The non-gate overlap region is located at the drain side, so the bottom channel near drain side is weakly controlled by the bottom gate. As a result, the drain potential can easily extend toward the channel through the bottom part of the channel region.

3. Conclusion

A two-dimensional analytical model for a GC DG MOSFET has been developed to investigate the effectiveness of graded channel design in suppressing the short channel effects. The model was
used to obtain surface potential, electric field, threshold voltage, DIBL and subthreshold slope of the device. The results so obtained have been compared with simulated results obtained from an ATLAS 3-D device simulator and are in good agreement. In UD devices, misalignment causes degradation in device characteristics for both DGD and DGS structures, while a DGS structure shows larger effect of gate misalignment in comparison to DGD configuration. GC architecture using a high-low doping profile causes a reduction in the gate misalignment effects for a DGD structure, whereas high-low doping profile causes increase in misalignment effects for DGS structure in comparison to UD devices. It was observed that the shift in the minimum surface potential is negligible for GC devices even when gate-misalignment increases for channel lengths down to 60nm. This clearly indicates that introducing a step-doping profile in the channel leads to a suppression of the gate misalignment effect and SCEs. It was also found that GC design leads to a reduction in peak electric field at the drain end, which reduces the impact ionization and hot carrier effects thus improving the hot carrier reliability of the device. The device characteristics are over-estimated about 0%–15% without considering the quantum and polysilicon effects for our analysis. The symmetrical DG (n⁺/n⁻) provides better immunity to the effects of gate misalignment in comparison with the asymmetrical DG (n⁺/p⁺) for both UD and GC architectures.

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Fig. 4. (a), (b) Backsurface potential variation with lateral direction for asymmetrical DG \((n^+/p^+)\) SOI for \(V_{DS} = 50\) mV, \(V_{CS} = 0\) V, \(L = 60\) nm, \(t_{ox1} = t_{ox2} = 2\) nm (a) UD DG SOI (b) GC DG SOI. (c), (d) Back surface electric field variation with lateral direction for asymmetrical DG \((n^+/p^+)\) SOI for \(V_{DS} = 50\) mV, \(V_{CS} = 0\) V, \(L = 60\) nm, \(t_{si} = 10\) nm, \(t_{ox1} = t_{ox2} = 2\) nm (c) UD DG SOI (d) GC DG SOI.

Appendix

The constants for front and the back surface potentials, used in the above equations are obtained by solving Eqs. (7)–(16) with all the boundary conditions.

\[
V_{1i} = \frac{s_{1i} \exp(-n_{1i}) (g_1 + g_2 - g_{3i} - g_{4i}) - \left(s_2 \sqrt{A_0} \sqrt{A_2} \right) - F_{1i}}{DR_{11}} \tag{A.1}
\]

\[
V_{2i} = \frac{-s_{1i} \exp(n_{1i}) (g_1 + g_2 + g_{3i} + g_{4i}) - \left(s_2 \sqrt{A_0} \sqrt{A_2} \right) - F_{1i}}{DR_{11}} \tag{A.2}
\]

\[
j_1 = \frac{-s_2 (g_5 + g_6 + g_7 + g_8) - \left(s_{11} \sqrt{A_{01}} \sqrt{A_{02}} (\exp(-n_3)) \right) - h_1}{DR_{12}} \tag{A.3}
\]

\[
j_2 = \exp(n_3)(s_2 - j_1 \exp(n_3)) \tag{A.4}
\]

\[
V_{3i} = \frac{s_{1} \exp(-n_{1i}) (g_1 + g_2 - g_{3i} - g_{4i}) - \left(s_3 \sqrt{A_0} \sqrt{A_2} \right) - F_{13}}{DR_{11}} \tag{A.5}
\]

\[
V_{4i} = \frac{s_{1} \exp(n_{1i}) (g_1 + g_2 + g_{3i} + g_{4i}) + \left(s_3 \sqrt{A_0} \sqrt{A_2} \right) + F_{13}}{DR_{11}} \tag{A.6}
\]
Fig. 5. (a), (b) Front surface potential variation with lateral direction for asymmetrical DG ($n^+/p^+$) SOI for $V_{DS} = 50$ mV, $V_{GS} = 0$ V, $L = 60$ nm, $t_s = 10$ nm, $t_{ox1} = t_{ox2} = 2$ nm (a) UD DG SOI (b) GC DG SOI. (c), (d) Front surface electric field variation with lateral direction for asymmetrical DG ($n^+/p^+$) SOI for $V_{DS} = 50$ mV, $V_{GS} = 0$ V, $L = 60$ nm, $t_s = 10$ nm, $t_{ox1} = t_{ox2} = 2$ nm (c) UD DG SOI (d) GC DG SOI.

\[ j_3 = \frac{-s_2 (g_5 + g_6 + g_7 + g_8) - (s_{11} \sqrt{A_{02}} \sqrt{A_{01}} \exp(-n_3))) - (\exp(-n_3)) F_{14}}{DR_{12}} \]  
(A.7)

\[ j_4 = \frac{s_2 (-g_5 + g_6 - g_7 + g_8) - (s_{11} \sqrt{A_{02}} \sqrt{A_{01}} \exp(n_3))) + (\exp(n_3)) F_{14}}{DR_{12}} \]  
(A.8)

where

\[ F_{1i} = \left[ \frac{\gamma \sqrt{A_{02}}}{\kappa} \left( \frac{A_{1i}}{A_{0i}} - \frac{A_{12}}{A_{02}} \right) \cosh(n_{12}) \cosh(n_3) + \frac{A_{1i}}{A_{0i}} \sinh(n_{12}) \sinh(n_3) + \frac{\gamma \sqrt{A_{02}}}{\kappa} \left( \frac{A_{12}}{A_{02}} + B_1 B_0 \right) \cosh(n_3) \right] \]

\[ h_1 = \exp(-n_3) \]

\[ \times \left( \sqrt{A_{02}} \sqrt{A_{01}} \left( \frac{B_1}{B_0} + \frac{A_{12}}{A_{02}} \right) \cosh(n_{12}) \cosh(n_{11}) \right) \]

\[ + A_{02} \left( \frac{B_1}{B_0} + \frac{A_{12}}{A_{02}} \right) \sinh(n_{12}) \sinh(n_{11}) \sqrt{A_{02}} \sqrt{A_{01}} \left( \frac{A_{11}}{A_{01}} \frac{A_{12}}{A_{02}} \right) \cosh(n_{11}) \]

\[ DR_{11} = -2 \left[ \frac{\gamma}{\kappa} \cosh(n_1) \left( \sqrt{A_{02}} \sinh(n_{11}) \cosh(n_{12}) \right) + \sqrt{A_{01}} \cosh(n_{11}) \sinh(n_{12}) \right] \]

+ $\sqrt{A_{02}} \sinh(n_3) \left( \sqrt{A_{02}} \sinh(n_{11}) \sinh(n_{12}) + \sqrt{A_{01}} \cosh(n_{11}) \cosh(n_{12}) \right)$
Fig. 6. (a), (b) $I_{DS}$–$V_{GS}$ curves for UD symmetrical DG ($n^+/n^+$) SOI for different Channel-doping concentration at $V_{DS} = 50$ mV (a) $m_a = 0$, (b) $m_a = 15$ nm. (c), (d) $I_{DS}$–$V_{GS}$ curves for GC symmetrical DG ($n^+/n^+$) SOI using $\square\square\square N_1 = 1 \times 10^{18}$ cm$^{-3}$, $N_2 = 1 \times 10^{17}$ cm$^{-3}$ and $\diamond\diamond\diamond N_1 = 2 \times 10^{18}$ cm$^{-3}$, $N_2 = 1 \times 10^{17}$ cm$^{-3}$ (c) $m_a = 0$ (d) $m_a = 15$ nm.

$$DR_{12} = -2 \left[ \frac{\gamma}{\kappa} \cosh(n_3) \left( \sqrt{A_{01}} \sinh(n_{11}) \cosh(n_{11}) + \sqrt{A_{01}} \cosh(n_{11}) \sinh(n_{11}) \right) \right]$$

$$F_{13} = \left[ \frac{\gamma \sqrt{A_{02}}}{\kappa} (D_1 - D_2) \cosh(n_{12}) \cosh(n_3) + A_{02} (D_1 - D_2) \sinh(n_{12}) \cosh(n_3) + \frac{\gamma \sqrt{A_{02}}}{\kappa} (D_2 + D_3) \cosh(n_3) \right]$$

$$F_{14} = \left[ \sqrt{A_{02}} \sqrt{A_{01}} (D_2 + D_3) \cosh(n_{12}) \cosh(n_{11}) + A_{02} (D_2 + D_3) \sinh(n_{12}) \sinh(n_{11}) + \sqrt{A_{02}} \sqrt{A_{01}} (D_1 - D_2) \cosh(n_{11}) \right]$$

$$g_1 = \frac{\gamma \sqrt{A_{02}}}{\kappa} \cosh(n_{12}) \cosh(n_3), \quad g_2 = A_{02} \sinh(n_{12}) \sinh(n_3),$$

$$s_{1i} = \phi_f + V_S + \frac{A_{1i}}{A_{0i}}, \quad g_{3i} = \frac{\gamma \sqrt{A_{0i}}}{\kappa} \sinh(n_{12}) \cosh(n_3),$$

$$g_{4i} = \sqrt{A_{0i}} \sqrt{A_{02}} \cosh(n_{12}) \sinh(n_3), \quad s_2 = \phi_f + V_D - \frac{B_1}{B_0},$$

$$g_5 = \frac{\gamma \sqrt{A_{02}}}{\kappa} \cosh(n_{12}) \sinh(n_{11}), \quad g_6 = A_{02} \sinh(n_{12}) \sinh(n_{11}).$$
Fig. 7. (a), (b) $I_{DS}$-$V_{GS}$ curves for UD asymmetrical DG ($n^+/p^+$) SOI with different Channel-doping concentration for $V_{DS} = 50$ mV (a) $m_a = 0$ (b) for $m_a = 15$ nm. (c), (d) $I_{DS}$-$V_{GS}$ curves for GC asymmetrical DG ($n^+/p^+$) SOI with $N_1 = 1 \times 10^{18} \text{cm}^{-3}$, $N_2 = 1 \times 10^{17} \text{cm}^{-3}$ and $\Delta N_1 = 2 \times 10^{18} \text{cm}^{-3}$, $N_2 = 1 \times 10^{17} \text{cm}^{-3}$ (c) $m_a = 0$ (d) $m_a = 15$ nm.

\[
g_7 = \frac{\gamma \sqrt{A_{01}}}{\kappa} \sinh (n_{12}) \cosh (n_{11}), \quad g_8 = \sqrt{A_{01} A_{02}} \cosh (n_{12}) \cosh (n_{11})
\]

\[
n_{11} = \frac{\sqrt{A_{00} L_m}}{2}, \quad n_3 = \frac{\gamma}{\kappa} m_a, \quad s_i = \phi_{fn} + V_S + D_i, \quad s_3 = \phi_{fn} + V_D - D_3.
\]

References


