Modeling of hetero-interface potential and threshold voltage for tied and separate nanoscale InAlAs–InGaAs symmetric double-gate HEMT

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ABSTRACT

This paper presents an approximate solution of a 2-D Poisson’s equation in the channel region, based on physical correspondence between MOSFET and HEMT, with the approximation that the vertical channel potential distribution is a cubic function of position to study not only tied gate but separate gate bias conditions as well. An analytical expression for both front and back heterointerface potential is derived and threshold voltage is obtained iteratively from the proposed potential model. The threshold voltage behavior for tied and separated double-gate HEMT is investigated for various device dimensions. The back gate effect of the separated double gate HEMT is investigated for the depleted back channel only. The results obtained are verified by comparing them with simulated and experimental results.

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1. Introduction

InP-based InAlAs/InGaAs high electron mobility transistors (HEMTs) are currently the fastest transistors operating in the millimeter-wave (30–300 GHz) and sub-millimeter-wave (300 GHz to 3 THz) frequency ranges [1], thus meeting the ever growing demand for MMIC’s in fields of satellite communications, high-speed wireless access and intelligent transportation systems. Since the introduction of FETs, reduction of gate-length ($L_g$) has been one of the basic thumb rules to enhanced RF performance. For $L_g$ below 100 nm, transconductance ($g_m$) starts degrading appreciably with decrease in $L_g$ [2,3]. This results in the onset of short-channel effects, mainly due to the inability of the structure to maintain a desired aspect-ratio ($L_g/d$) [4,5] as the vertical scaling is limited by several physical limitations like the emergence of gate tunnel current for reduced schottky layer thickness and the loss of mobility with the reduction of the spacer layer thickness [6–9]. However, the cut-off frequency ($f_t$) continues to increase, as degradation in transconductance is overcome by the reduction in total capacitance, but the maximum frequency of oscillation ($f_{max}$) degrades as unloaded voltage gain ($g_m/g_d$) of the device decreases [10,11]. For 25 nm T-gate InAlAs/InGaAs pseudomorphic HEMT, $f_t$ is observed to be 562 GHz, while $f_{max}$ is only 330 GHz [1].

The frequency performance could be enhanced further by using alternative approaches such as (a) multilayer cap technology to reduce parasitic resistance [12], (b) graded InGaAs channel [13] or InAs in the channel [14] to enhance carrier mobility. Kim and del Alamo [14] has optimized single gate InAs Pseudomorphic HEMT for higher $f_t$ and $f_{max}$ by (a) using InAs between InGaAs layers in the channel (b) varying the distance between the gate edge and the cap recess, (c) increasing the gate stem height and using multilayer cap technology to reduce parasitic resistance and (d) reducing the schottky layer thickness and channel thickness to 4 nm and 10 nm, respectively, which results in a record $f_t$ of 628 GHz for 30 nm gate length HEMT and a best combination of $f_t$ and $f_{max}$ of 557 GHz and 718 GHz, respectively, for 50 nm gate length in any transistor technology. Though RF performance is raised but the factors like emergence of gate leakage current through schottky barrier below 8–10 nm and the breakdown reliability of using InAs in the channel may be detrimental to the overall device performance as the relative narrow band gap of InAs (~0.36 eV), may subject the device to several impact ionization related non-idealities, some of which may involve trapping of holes generated by impact ionization.

So, an alternative solution based on an evolution of the standard HEMT design has to be considered. As double-gate technology in MOSFET has provided superb short channel immunity, high transconductance, improved charge control in the channel, thus providing a solution for further gate-length scaling [15]. Similarly in HEMT, the double-gate structure has been proposed and fabricated using transferred substrate technique by Wichmann et al. [16] in order to improve short channel effects thus enhancing $f_t$ and $f_{max}$ of the device. The reduction in $g_d$ is also observed due to removal of buffer layer and higher carrier confinement in double gate-HEMT (DGHEMT). This noticeable combined effect of higher $g_m$ and lower $g_d$ results in extremely high intrinsic unloaded voltage...
gain $g_m/g_d$ and thus an improved value of $f_{max}$ [10]. DGHEMT has also demonstrated improved noise behavior over its single gate counterpart in terms of intrinsic $P$ and $R$ noise parameters and extrinsic $N_{F_{min}}$, $G_{min}$ and $R_{n}$ noise parameters [17]. In that case DGHEMT technology has become one of the viable solutions for reducing short channel effects and thus enhancing the device performance, irrespective of expensive and complicated technology used in the fabrication of double gate device.

While the previous papers [10,16] have focused on the experimental and Monte-Carlo Simulator results, this paper presents a conference presentation [18] in which the effect of channel thicknesses. The paper is an updated and extended version of our recent definition of

devices get complicated further due to the co-existence of the front and the back channels, so a 2-D DGHEMT.

(a) Cross-sectional view of DGHEMT. (b) Conduction Energy Band Diagram of DGHEMT.

Fig. 1a shows the schematic structure of DGHEMT with two identical $T$-gates, one at the top and other at the bottom, followed by an undoped InAlAs schottky layer of thickness $d_s$, a doped layer of thickness $d_o$, with the doping concentration $N_d$, to provide necessary 2-DEG sheet charge density and an undoped InGaAs spacer layer of thickness $d_s$. Thus the total thickness of InAlAs is taken as $d = d_s + d_o + d_i$ on both side of unintentionally doped InGaAs layer of thickness $d_i$ to form the 2-DEG channel. Table 1 lists various parameters of ternary semiconductors InAlAs and InGaAs used in simulation and modeling of various devices. Fig. 1b shows the conduction band energy diagram of DGHEMT under two schottky gates. Here, only symmetric DGHEMT is considered, in which both the heterostructure are symmetrical in every aspects including delta-doping, nature of schottky-barrier and the dimensions of various layers used in the formation of heterostructures.

2.2. Flat-band voltage in HEMT: correspondence between MOSFET and HEMT

The concept of flat band voltage ($V_{fb}$) in HEMT is based on the physical correspondence between the MOSFET and the HEMT as from electrostatic point of view, the two devices are rather similar. The modulation-doped structure of Fig. 2a may be viewed as a pseudo-MOS structure, where InAlAs plays the role of insulator, and the InGaAs mimics the thin Si body. Such physical correspondence has been widely reported by several authors [19–26] not only for the analytical solutions but for the circuit designs and noise analysis too. Of recently, HEMTs have been bench marked against CMOS [7] to further sustain the Moore’s Law as Si-based devices will reach 10 nm critical gate lengths by 2011, which is widely believed as the ultimate CMOS scaling limit.

In general, flat-band voltage is defined as the gate voltage at which all the carriers are depleted in the channel ($n_t = 0$) and is given by Khondker et al. [21]

$$
V_{fb} = \phi_b - \Delta E_c - \frac{q \cdot N_d}{\varepsilon_A} \cdot \frac{d_s^2}{d_s^2} \left( 1 + \frac{2}{d_i} \frac{d_i}{d_s} \right) + E_f
$$

(1)

where $\phi_b$ is schottky barrier height, $q$ is magnitude of electronic charge, $\Delta E_c$ is conduction band discontinuity, $\varepsilon_A$, $N_d$ are permittivity and doping in InAlAs, respectively, and $d_s$, $d_i$ are thickness of doped and schottky layer, respectively. The non-linear relationship between the position of Fermi-level $E_f$ and the 2-DEG charge concentration ($n_t$) as established by DasGupta and DasGupta [26] is given as,

$$
E_f = k_1 - k_2 \cdot n_t^{1/2} + k_3 \cdot n_t
$$

(2)

where $k_1, k_2$, and $k_3$ are constant. The value of $E_f$ for $n_t = 0$ is denoted by $E_f^0$ and is equal to $k_1$, ($k_1$ is calculated as $-0.139547$ V at 300 K) [26], which when interpreted physically means that conduction band edge is above the Fermi-level by $-0.139547$ V as $E_f$ is the measured from the conduction-band edge at the hetero-interface as shown in Fig. 2b.

Table 1: List of InAlAs/InGaAs ternary semiconductor parameters.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Material</th>
<th>In$<em>{0.52}$Al$</em>{0.48}$As</th>
<th>In$<em>{0.53}$Ga$</em>{0.47}$As</th>
</tr>
</thead>
<tbody>
<tr>
<td>Indium concentration (mole fraction)</td>
<td>0.52</td>
<td>0.53</td>
<td></td>
</tr>
<tr>
<td>Band gap ($E_g$) (eV)</td>
<td>1.47</td>
<td>0.74</td>
<td></td>
</tr>
<tr>
<td>Electron affinity ($\chi$)</td>
<td>4.20</td>
<td>4.72</td>
<td></td>
</tr>
<tr>
<td>Conduction band offset ($\Delta E_c$) (eV) (relative to In$<em>{0.52}$Al$</em>{0.48}$As)</td>
<td>0.52</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Relative permittivity ($\varepsilon_r$)</td>
<td>12.47</td>
<td>13.895</td>
<td></td>
</tr>
<tr>
<td>Electron mobility ($\mu_e$) (cm$^2$/Vs)</td>
<td>4100</td>
<td>11,400</td>
<td></td>
</tr>
<tr>
<td>Saturation velocity (cm/s)</td>
<td>$2.1 \times 10^7$</td>
<td>$2.63 \times 10^7$</td>
<td></td>
</tr>
<tr>
<td>Electron effective density of states (cm$^{-3}$)</td>
<td>$5.30 \times 10^{17}$</td>
<td>$2.18 \times 10^7$</td>
<td></td>
</tr>
<tr>
<td>Hole effective density of states (cm$^{-3}$)</td>
<td>$1.09 \times 10^{19}$</td>
<td>$8.44 \times 10^{18}$</td>
<td></td>
</tr>
</tbody>
</table>
When the gate voltage \( V_g \) is increased above \( V_{fb} \) (\( V_g - V_{fb} \)) is partitioned between the \textit{InAlAs} layer and the \textit{InGaAs} layer [21]. For \( V_g > V_{fb} \), the additional drop across \textit{InAlAs} and its dependence on \( V_g \) is as follows:

\[
V_f^2 - V_2 = V_g - V_{fb} - \psi_s
\]  
(3)

where \( \psi_s \) is the band bending at the heterointerface in the \textit{InGaAs}. Further, the electric field at the heterointerface on \textit{InGaAs} side is given by

\[
E_c = \frac{C_A}{\varepsilon_c} (V_f^2 - V_2) = \frac{C_A}{\varepsilon_c} (V_g - V_{fb} - \psi_s),
\]  
(4)

where \( C_A = \frac{q}{\varepsilon} \) is the depletion capacitance and \( \varepsilon_c \) is the permittivity of \textit{InGaAs}. This expression is similar to that obtained in MOSFET. The band bending \( (\psi_s) \) is expressed as [27,28]

\[
\psi_s = \left( \frac{q}{\varepsilon_c} \right) \cdot x_{av} \cdot n_i + \frac{q \cdot N_A \cdot W^2}{2 \cdot \varepsilon_c}
\]  
(5)

where \( x_{av} \) is the average distance of 2-DEG from the interface, \( W \) is the depletion width and \( N_A \) is the ionized unintentional doped density in \textit{InGaAs} region. The first term is the potential drop across 2-DEG and the second one is the usual band bending due to \( N_A \). In sub-threshold region of operation, \( n_i \) is negligible compared to total depletion charge, i.e., \( n_i \ll N_A \cdot W \). So, considering this analogy and defining the onset of threshold voltage when the band bending equals twice the fermi-potential in the channel [29], we have formulated our model in the next section.

### 2.3. Model formulation

In order to arrive at a precise definition of threshold voltage and potential distribution, the Poisson equation has been solved in the channel region under the gate as shown in Fig. 1. The 2-D Potential distribution \( \Psi(x, y) \) can be obtained by solving 2-D Poisson equation, given by

\[
\frac{\partial^2 \psi(x, y)}{\partial x^2} + \frac{\partial^2 \psi(x, y)}{\partial y^2} = \frac{qN_A}{\varepsilon_c}
\]  
(6)

where \( 0 < x < L_g \) and \( 0 < y < d_c \) in the channel region. In sub-threshold region mobile charge density \( (n_i) \) term is ignored which restricts our analysis to subthreshold regime only.

Although, a symmetric potential distribution (tied gate bias condition) can be represented well by a second order polynomial but for asymmetric potential distribution as the case for separate gate bias condition a cubic-polynomial yields better results. So a cubic potential distribution along vertical direction is considered to study both tied and separate gate bias conditions [30]:

\[
\psi(x, y) = a(x) + b(x)y + c(x)y^2 + d(x)y^3
\]  
(7)

The coefficients \( a(x), b(x), c(x), \) and \( d(x) \) are functions of \( x \) only and are solved with following boundary conditions, obtained from the MOSFET analogy as discussed in Section 2.2.

\[
\psi(x, 0) = \psi_f(x)
\]

\[
\psi(x, d_c) = \psi_b(x)
\]

\[
\left. \frac{d\psi(x, y)}{dy} \right|_{y=0} = \frac{C_A}{\varepsilon_c} \left[ \psi_f(x) - (V_{fb} - V_{bg}) \right]
\]

\[
\left. \frac{d\psi(x, y)}{dy} \right|_{y=d_c} = \frac{C_A}{\varepsilon_c} \left[ (V_{bg} - V_{fb}) - \psi_b(x) \right]
\]  
(8)

where \( \psi_f(x) \) and \( \psi_b(x) \) are the front and back surface potentials, \( C_A \) is the depletion capacitance of \textit{InAlAs} layers, \( V_f \) and \( V_{bg} \) are the front and back gate voltages, respectively. The flat band voltage \( (V_{fb}) \) is same for both front and back gates as the \textit{InAlAs} dimensions (Schottky layer, delta-doped layer, doping concentration, spacer layer) and gate metal is considered same for both heterostructures. Separate solutions are obtained one for tied gate when same voltage is applied to both front and back gate i.e., \( V_f = V_{bg} \) and the other for separate gate configuration when a fixed voltage is applied to one of the gate and a variable input is applied to the other gate i.e., \( V_f \neq V_{bg} \).

Solving Eq. (7) with boundary conditions given in Eq. (8), the values of the coefficients \( a(x), b(x), c(x) \) and \( d(x) \) are obtained and by rearranging them we have,

\[
\psi(x, y) = \psi_f(x) \left\{ 1 + \frac{C_A}{\varepsilon_c} \cdot y \left( \frac{3}{d_c^2} + \frac{2}{\varepsilon_c \cdot d_c} \right) \cdot y^2 + \frac{2}{\varepsilon_c \cdot d_c} \cdot y^3 \right\} + \psi_b(x) \left\{ \left( \frac{3}{d_c^2} + \frac{C_A}{\varepsilon_c \cdot d_c} \right) \cdot y^2 - \frac{2}{\varepsilon_c \cdot d_c} \cdot y^3 \right\}
\]  

\[
- \frac{C_A}{\varepsilon_c} \cdot V_f^2 \cdot y + \frac{C_A}{\varepsilon_c \cdot d_c} \cdot (2 \cdot V_f^2 - V_{bg}) \cdot y^2 - \frac{C_A}{\varepsilon_c \cdot d_c} \cdot (V_f^2 - V_{bg}) \cdot y^3
\]  
(9)

where \( V_f^2 = V_f - V_{fb} \) and \( V_{bg}^2 = V_{bg} - V_{fb} \).

To find a correlation between the unknown variables \( \psi_f(x), \psi_b(x), \) and \( V_f^2, \ V_{bg}^2 \), the vertical potential plot in sub-threshold region is studied using Atlas simulator [31]. It is found that in the subthreshold region potential distribution along vertical y-axis is a straight line in the channel and shows a parallel shift to the gate-voltage. Using the similar approach as followed by Suzuki and Sugii [32] and Han et al. [30] and assuming the potential in
InAlAs as a straight line, the following correlation is obtained between \( \psi_f(x) \) and \( \psi_d(x) \):

\[
\psi_f(x) - \psi_d(x) = \frac{d_c}{d_{eq}} (V_{fs} - V_{bg})
\]

(10)

where \( d_{eq} = 2 \cdot \frac{d}{d} + d_c \).

It may be noted that the above relation is valid only under the sub-threshold regime. Further, this 1-D approximation might cause error in 2-D potential distribution, but this error is effectively minimized by thin channel double-gate effect in DG devices.

Substituting Eq. (10) into Eq. (9) we get,

\[
\psi(x,y) = \psi_f(x) + \frac{C_A \cdot \psi_f(x) - V_{fs}}{e_C} \cdot y + \frac{e_d \cdot d_{eq} \cdot (2 \cdot V_{fs} - V_{bg} - \psi_f(x)) - (3 \cdot e_C \cdot d + e_d \cdot d_c) \cdot (V_{fs} - V_{bg})}{e_C \cdot d - d_c \cdot d_{eq}} \cdot y^2
\]

(11)

To obtain an expression of potential at any arbitrary depth in the channel region, 1-D potential distribution analysis at an arbitrary depth \( y_a \) is defined as \( \psi_f(x) = \psi(x, y = y_a) \). The front surface potential is obtained in terms of \( \psi_f(x) \) from Eq. (11) by putting \( y = y_a \) as:

\[
\psi_f(x) = \frac{1}{P_{ym}} \left\{ \psi_f(x) + \frac{C_A \cdot y_a}{e_C} \cdot V_{fs} - \frac{C_A \cdot y_a^2}{e_C \cdot d_c} \cdot V_{fs} + \frac{V_{fs} - V_{bg}}{d_c \cdot d_{eq}} \cdot y_a^2 \right\}
\]

(12)

where \( P_{ym} = 1 + \frac{C_A \cdot y_a}{e_C} - \frac{C_A \cdot y_a^2}{e_C \cdot d_c} \).

Using the above expression in Eq. (11), we get,

\[
\psi(x, y) = \frac{P_y}{P_{ym}} \left\{ \psi_f(x) + \frac{C_A \cdot y_a}{e_C} \cdot V_{fs} - \frac{C_A \cdot y_a^2}{e_C \cdot d_c} \cdot V_{fs} + \frac{V_{fs} - V_{bg}}{d_c \cdot d_{eq}} \cdot y_a^2 \right\} - \frac{C_A \cdot y_a}{e_C} \cdot V_{fs} + \frac{C_A \cdot y_a^2}{e_C \cdot d_c} \cdot V_{fs} - \frac{V_{fs} - V_{bg}}{d_c \cdot d_{eq}} \cdot y_a^2
\]

(13)

where \( P_y = 1 + \frac{C_A \cdot y_a}{e_C} - \frac{C_A \cdot y_a^2}{e_C \cdot d_c} \).

By substituting Eq. (13) into Eq. (6) and putting \( y = y_a \), the 2-D Poisson’s equation can be reduced to a simple 1-D second-order non-homogeneous differential equation for the potential distribution along an arbitrary depth \( y_a \) in the InGaAs channel as:

\[
\frac{\partial^2 \psi_f(x, y)}{\partial x^2} + \frac{\partial \psi_f(x, y)}{\partial y} = \frac{q \cdot N_A}{e_C} \cdot \left( \frac{V_{fs} - V_{bg}}{d_c \cdot d_{eq}} \right) \cdot y_a
\]

(14)

where \( \lambda_y \) is represented by

\[
\lambda_y = \sqrt{\frac{e_C}{2} \cdot P_{ym} \cdot d \cdot d_c}
\]

(15)

Solving Eq. (14) with boundary conditions:

\[
\psi_f(0) = V_{th} \quad \text{and} \quad \psi_f(L_g) = V_{th} + V_d
\]

(16)

The general solution of the potential for an arbitrary depth \( y_a \) can be written as:

\[
\psi_f(x) = A_y \cdot \exp(x/\lambda_y) + B_y \cdot \exp(-x/\lambda_y) - \chi_y
\]

(17)

where

\[
A_y = \left\{ \frac{\zeta_0 - \zeta_2 \cdot \exp(-L_g/\lambda_y)}{1 - \exp(-2 \cdot L_g/\lambda_y)} \right\} \cdot \exp(-L_g/\lambda_y)
\]

\[
B_y = \left\{ \frac{\zeta_0 - \zeta_2 \cdot \exp(-L_g/\lambda_y)}{1 - \exp(-2 \cdot L_g/\lambda_y)} \right\}
\]

\[
\chi_y = \frac{q \cdot N_A \lambda_y^2}{e_C} + \frac{V_{fs} - V_{bg}}{d_c \cdot d_{eq}} \cdot y_a
\]

As the above solution is at any arbitrary position \( y_a \) in the entire channel, so the 2-D channel potential \( \psi(x, y) \) can be obtained by replacing \( y_a \) in \( \chi_y \) with \( y \), i.e.,

\[
\psi(x, y) = A_y \cdot \exp((L_g - x)/\lambda_y) + B_y \cdot \exp((x)/\lambda_y) - \chi_y
\]

(18)

As mentioned above, the error due to 1-D approximation (10) is minimized due to thin channel double gate effects. Though this restricts the results matching with simulated results for \( L_g > 2 \cdot d_c \). Also as, \( L_g > 2 \cdot d_c \) is the commonly used design rule in the DG structures; therefore, the model is valid for reasonable device dimensions. So for \( d_c = 10 \text{ nm} \) model is valid for \( L_g > 20 \text{ nm} \).

3. Results and discussion

The analytical results obtained are compared with Atlas Simulated results. For simulation the parameters considered for InAlAs and InGaAs are listed in Table 1, the delta-doping is realized through a thin uniformly doped layer of thickness \( d_{as} \), with the doping concentration \( N_d \) and the source and drain electrodes are limited to the channel region as our analytical model do not consider parallel conduction in the device. The simulated value of threshold voltage is obtained from \( I_{ds} = V_g \) characteristics by extrapolating the \( I_D \) versus \( V_g \) curve to zero current (Quadratic Extrapolation Method) [33].

3.1. Tied symmetric DGHEMT

Tied Symmetric-DGHEMT (TS-DGHEMT) device works as a conventional two port system as same gate-bias \( (V_{fs} = V_{bg}) \) is applied to both of the gate electrodes. This results in similar potential profile for both front \( (y = 0) \) and back \( (y = d_c) \) channel cases, which are obtained from Eq. (18). Therefore, the threshold voltage \( (V_{th}) \) can be defined by minima of either front or back channel potential. The minimum potential along x-direction at given depth y is calculated from Eq. (17) by putting \( V_{fs} = V_{bg} \) i.e.,

\[
\psi_{min}(y) = 2 \cdot \sqrt{A_y \cdot B_y - \chi_y}
\]

(19)

And, \( V_{th} \) is obtained by solving \( \psi_{min}(0) \) \( \neq 2 \cdot \phi_t \) [29], or \( \psi_{min}(d_c) \neq 2 \cdot \phi_t \), where \( \phi_t \) is the fermi-potential in the channel. Fig. 3a and b shows the plots of the heterointerface potential along normalized channel length \( (x/L_g) \) for \( d_c = 10 \text{ nm} \) and \( d_c = 30 \text{ nm} \) for different gate-lengths at two different drain bias, viz. 0.05 V and 0.01 V. It can be seen from the graphs that shorter gate length and thicker channel shows prominent variation in minimum channel potential which is because of onset of short-channel effects at the shorter gate lengths and thicker channel. This can be explained by the concept of aspect ratio \( (\gamma) \) defined as \( \gamma = L_g/d, \) an important
parameter indicating the presence of short channel effects in a device. The body factor $k$ given by Eq. (15), which at $y=0$ or $d_c$ becomes $\sqrt{\frac{2}{\epsilon_e}} d \cdot d_c$. The scaling of gate length leads to lower values of aspect ratio which results in greater short-channel effects in the device. However, with the scaling of channel thickness the aspect ratio increases, which is an indication of the improved short-channel effects in the device. Therefore, for a particular gate length, thinner channels are favorable for the improve sub-threshold behavior.

Fig. 4 shows the variation of threshold voltage with gate-length for various channel thickness. The modeled results for $d_c = 20$ nm has also been validated with the experimental results [10] and the close matching of the results proves the validity of our model. As it can also be seen from the figure that gate-length scaling leads to threshold voltage roll-off due to oncoming of short channel effects into the device and this roll-off is greater for higher $d_c$. The graph also shows that for $d_c = 30$ nm, the results start deviating from the simulated data as the gate length approaches the limit of $2 \cdot d_c$. It may be noted that for a particular gate length, device having thicker channel have more negative threshold voltage. This is because thicker channel, besides having greater short-channel effects also results in the increased distance between the gates (front and back) which lead to the inefficient depletion of the channel charge.

3.2. Separated symmetric DGHEMT

In Separated Symmetric-DGHEMT (SS-DGHEMT) two gates are biased independently ($V_{fg} \neq V_{bg}$). A fixed bias is applied to one of the gate (back gate) and a variable input is applied to the other gate (front gate). Under such conditions, the device operates as a three-port system thus offering novel possibilities like mixing applications. As discussed earlier, our model for separate gate bias is valid under the condition, $V_{bg} < V_{fb}$ i.e., back channel does not exist otherwise it would have screen out the effect of back gate. For a fixed value of $V_{bg}$, both front and back channel potentials are obtained by putting $y = 0$ for front heterointerface potential and $y = d_c$ for back heterointerface potential in Eq. (18). As back gate voltage is well below the flat band voltage, therefore, the minimum potential along $x$-direction at $y = 0$ (front heterointerface) determines the threshold voltage condition that is obtained by solving $\psi_{min}(0) = 2 \cdot \phi_f$.

Fig. 5 shows the drain induced barrier lowering (DIBL), defined as difference in threshold voltage at $V_{ds} = 0.5$ V and $V_{ds} = 0.01$ V, with gate-length for various channel thickness. It can be seen that shorter gate-lengths and thicker $d_c$ shows higher DIBL effects and for a particular gate-length thinner channel are favorable for the improved subthreshold behavior of the device.
Fig. 6a and b plots the effect of back gate voltage for $V_{bg} = -0.7$ V and $-0.9$ V on the front heterointerface potential along normalized channel length ($x/L_g$) at two different channel thickness ($d_c = 10$ nm and $30$ nm) and for two gate lengths ($L_g = 100$ nm, $70$ nm). It can be seen from the graphs that the effect of back gate voltage is slightly more in case of thinner channel ($d_c = 10$ nm). Also the effect of back gate bias is independent of gate length scaling as for both $100$ nm and $70$ nm gate length the variation in the back gate bias shows similar variation on potential profile. Fig. 7a and b plots the back heterointerface potential along normalized channel length ($x/L_g$) at $V_{bg} = -0.7$ V and $-0.9$ V for $L_g = 100$ nm and $70$ nm for different channel thickness ($d_c = 10$ nm and $30$ nm) at $V_{ds} = 0.5$ V and $V_{bg} = -0.7$ V shows the usual variation in heterointerface potential for different back gate voltages.

The variation in threshold voltage with back gate bias ($V_{bg}$) for different channel thickness is plotted in Fig. 8 for different gate length ($L_g = 100$ nm and $70$ nm). With the increase in channel thickness the back gate bias effect decreases which is evident from the slope of the lines. The decrease in slope indicates the diminished effect of the back gate. The variation for $70$ nm gate length also shows similar variation in threshold voltage with back gate bias for different channel thickness. However, gate length variation shows almost negligible effect as curves for both $100$ nm and $70$ nm although having different values of threshold voltage, have same slope of variation of threshold voltage. Also for both gate lengths, an enhanced back gate effect is observed for thinner channel only.

Further, Fig. 8 illustrates the flexibility of DGHEMT with separate gate control that can be operated both in quasi-enhancement as well as in depletion mode on the same wafer and with the same technological process just by changing the back gate bias condition. Fig. 8 also shows that for a particular gate-length DGHEMT having thinner $d_c$ turns on first to enhancement mode as compared to the one having thicker $d_c$. This is again due to the better back gate effect at smaller channel thickness. Thus, SS-DGHEMT devices can have threshold voltage in a wide range by the virtue of the fixed bias applied to one of the gates which makes the device to operate both in quasi-enhancement and/or depletion mode just by changing the fixed gate bias condition.
4. Conclusions

An analytical subthreshold model based on physical correspondence between MOSFET and HEMT is proposed for DGHEMT with the approximation that the vertical channel potential distribution is a cubic function of position as cubic polynomial yields better results to study both tied gate and separate gate bias than second order polynomial. Expression for heterointerface potentials is derived and threshold voltage is obtained iteratively, both for tied and separate gate operations. The subthreshold behavior of the device has been studied for various gate-length and channel thicknesses. It is observed that for a particular gate-length thinner $d_g$ are favorable for improved short-channel effects. In the case of SS-DGHEMT, analysis has been done when the back channel has been depleted otherwise it would have screened out the effect of back gate. The back gate effect on the device characteristics is found out to be more prominent for thinner $d_g$; both quasi-enhancement and depletion mode operation of SS-DGHEMT is observed just by changing the fixed gate bias condition. This presents a potential advantage of SS-DGHEMT as a flexible device capable of operating in both modes without any technological/fabrication changes.

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